Development of a Grid Emulator for Network Integration Studies

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Declaration

This dissertation is submitted to the Department of Electrical Engineering, University of Cape Town, in complete fulfillment of the requirements for the degree of Master of Science in Electrical Engineering. It has not been submitted before for any degree or examination at this or any other university.

"I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own."

Akrama Khan

8th of May 2014

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Countless thanks to Almighty Allah, the creator of this universe. The Omnipotent, the Omnipresent, the most Merciful & Compassionate, the worthy of all praises. His will and blessings enabled me to complete this thesis successfully.

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Abstract

The economic and environmental side effects of fossil fuels have forced governments and authorities to investigate sustainable solutions. Main interest is focused on environment friendly benefits, provided by renewable energy sources. The growth rate of these energy sources has increased remarkably in the past few years. Correspondingly the research and development in the field of power electronics has also increased, especially in medium voltage and high power grid connected systems.

The grid behaviour of the renewable energy systems is heavily influenced by the control techniques of these systems. For further development of these control methods the most basic and conventional way is to simulate, test and prove the system performance on a down-scaled lab test bench. The objective of this thesis is to develop a laboratory test bench grid emulator for network integration studies. Design and performance are investigated by introducing several kinds of unbalanced voltage conditions to test the behavior of connected systems. Voltage dips and swells are implemented to test the system's performance.

This laboratory grid emulator is rated up to nominal power of 30 kW and can handle up to 0.5-1.5 times nominal voltage peaks. The behavior of both grid side and load side converters is analyzed in detail. Space vector voltage oriented control technique is implemented and PI controller gains are tuned accordingly. National Instruments PXI controller was used for hardware implementation. The experimental set up was assembled which proved to be a test system for the laboratory. A step by step approach is used for the filter design according to the system parameters.

It is found that unbalance can be generated and controlled with the help of dual vector sequence extraction technique. Furthermore, a detailed comparison is done between the two-level and the three-level converters and it shows that the three-level converter is more efficient with less voltage magnitude deviation and low spectrum distortion.

Certain limitations were encountered which are discussed and addressed in the thesis.

Table of Contents

List of Figures

List of Abbreviations

FRT	-	Fault Ride Through
LVRT	-	Low Voltage Ride Through
PI	-	Proportional Integral
UPF	-	Utility Power Factor
NPC	-	Neutral Point Clamped
VSI	-	Voltage Source Inverter
VSC	-	Voltage Source Converter
DFIG	-	Doubly Fed Induction Generator
PMSG	-	Permanent Magnet Synchronous Generator
PXI	-	*PC Extensions for Instrumentation*
THD	-	*Total Harmonic Distortion*
IEC	-	International Electrotechnical Commission
ANSI	-	*American National Standards Institute*
PWM	-	Pulse Width Modulation
SVPWM	-	Space Vector Pulse Width Modulation
VOC	-	Voltage Oriented Control
PLL	-	Phase Locked Loop
SCB	-	Shielded Connector Board

PCB	-	Printed Copper Board
SVM	-	Space Vector Modulation
L.V.	-	Low Voltage
Z_b	-	Base Impedance of the filter

List of Symbols

V_m	-	peak voltage
v_s	-	phase voltage
ω	-	angular frequency
$\vec{V}_{\text{ref}}$	-	reference vector
T_s	-	dwell time
v_i	-	inverter voltage
i_i	-	inverter current
c	-	voltage drop across filter capacitance
i_c	-	current across filter capacitance
v_g	-	grid voltage
L_i	-	filter inductance on inverter side
R_i	-	inverter side parasitic resistance
C_f	-	filter capacitance
L_g	-	filter inductance on grid side
R_g	-	grid side parasitic resistance
H_{LCL}	-	transfer function of an LCL filter
P_{series}	-	power loss in series damping resistance

$P_{parallel}$	-	power loss in parallel damping resistance
v_{α}	-	α-axis voltage
v_{β}	-	β-axis voltage
v_{d}	-	d-axis voltage
v_{d}^{+}	-	d-axis positive sequence voltage
v_{d}^{-}	-	d-axis negative sequence voltage
v_{q}	-	q-axis voltage
v_{q}^{+}	-	q-axis positive sequence voltage
v_{q}^{-}	-	q-axis negative sequence voltage
i_{g}	-	grid current
$L(s)$	-	transfer function of lead-lag block
Φ_{max}	-	maximum lead angle
k_{d}	-	gain of lead-lag transfer function
T_{d}	-	time constant
D_{z}	-	zero damping factor
D_{p}	-	pole damping factor
L_{b}	-	base inductance
C_{b}	-	base capacitance
E_{n}	-	line-to-line voltage

P_n	-	rated power
Δi	-	ripple current
f_s	-	switching frequency
F_{res}	-	resonant frequency
C_{min}	-	minimum capacitance
G_{ry}	-	closed loop transfer function
G_{MO}	-	transfer function for modulus optimum technique
G_{PI}	-	transfer function for the PI controller
$G_{control}$	-	transfer function for the control algorithm
$G_{converter}$	-	transfer function for the converter
G_{Filter}	-	transfer function for the filter
$G_{sampling}$	-	transfer function for the sampling data
$G_{current}$	-	transfer function for the current loop
G_{cap}	-	transfer function for the capacitor
K_p	-	proportional gain
K_i	-	integral gain
V_{CE}	-	collector emitter voltage
C_{CE}	-	collector emitter capacitance
R_{CE}	-	collector emitter resistance
R_c	-	parasitic resistance of the capacitor

I_g	-	grid current
ω_n	-	fundamental frequency
ω_{sw}	-	switching frequency
h_{sw}	-	switching frequency harmonic h_{sw}

CHAPTER 1

INTRODUCTION

1.1. Background

Energy has been harnessed from natural sources for centuries. Sunlight was used to heat water, wood for cooking and light, wind for sailing ships and grinding mills. As the energy demand increased, fossil fuels became the main source. Nevertheless, the rapid depletion of fossil fuels over the years together with the continuous increase in price and pollution prompted the attention of society towards more sustainable energy solutions. Consequently, clean energy provided by renewable sources have become of significant interest. Different renewable sources include hydropower, solar, wind, geothermal and biomass.

Although all these renewable energy technologies are emerging, wind and solar power technology are becoming most prominent. However, wind and solar power are ultimately derived from unpredictable natural resources so their outputs vary in their availability over time. This raises important issues when integrating larger amounts of renewable energy sources into an interconnected power system [1].

Wind generation is becoming a fast growing renewable source of electricity supply due to the increase in demand and has low emission production electricity in comparison to fossil based generation. Offshore wind farms are becoming popular due to space availability for the turbines. Wind power is a distributed energy generation source and therefore offers more economic and ecological advantages. However, its intermittent nature results in adverse effects on the stability of the network, particularly when the penetration level increases [2].

1.2. South Africa Energy Mix and Wind Power Development

Wind power in South Africa (S.A.) has moved from the planning to the execution phase, and is becoming one of the most vibrant new wind markets globally. S.A. is blessed with excellent

wind resources. After taking a decade to install the first 10 MW of wind power, the industry is currently developing between 3,000 MW and 5,000 MW of wind power, of which 636 MW is under construction and a further 562 MW approaching financial close. In addition, there is a long term energy blueprint giving wind a significant allocation, about 9,000 MW of new capacity in the period up to 2030. Wind power in S.A. is currently sold competitively at around ZAR 0,90/kWh (EUR 0.075 / 0.1 USD). The power purchase agreement (PPA) counterpart to wind developers is almost invariably Eskom, backed by the South African government. The industry in S.A. is in a very rapid growth phase. While some set-backs are likely, it seems quite certain that the country is moving towards a large wind industry with in excess of 5,000 MW installed within 15 years, and possibly much sooner. The integrated resource plan (IRP) mandates a total of 8,400 MW by 2030 and with the early signs of market development across southern Africa, S.A. could very well evolve into the hub for manufacturing and development that the industry has been looking forward to for many years [3].

To reach this target, continuous growth of wind power requires new technologies in the field of power electronics, especially in grid connected systems. The classical configuration of grid connected energy systems usually comprises two parts. The first part on the input side includes a power conditioner to boost the rectified voltage from the source and on the output side an inverter to convert and adapt this accumulated energy. However, the first part depends on the type of renewable energy source to be interlinked, while the output side remains the same.

Regardless of the load variation, the uninterrupted flow of energy from the grid to the load must be ensured. Moreover, different standards should be defined to limit the injection of harmonics into the grid. These requirements can only be achieved by continuous progress in the field of power electronics, especially in different converter topologies and their control strategies.

For low power systems a classical two-level converter is typically used between the generator and grid sides. However, for wind turbines with high power ratings special converters have been designed. These converters are emerging rapidly in the market and are becoming

industrial standards and are well accepted for high power medium voltage applications, and are called multilevel converters.

1.3. Wind Power Integration

Wind energy is perhaps the most mature of the various renewable energy technologies and has recently gained much favour worldwide. Proposals for wind developments in the hundreds of MWs are currently being considered. Interconnection of these developments into the existing utility grid poses significant challenges.

The existing targets for wind power anticipate quite a high level of penetration of wind power in many countries. It is theoretically possible to integrate very large amounts of wind capacity in power systems , however the limits are determined by cost and the need for energy storage or dispatch able generation sources to deal with the intermittent nature of wind power. So far the integration of wind power into regional power systems has mainly been studied on theoretical basis, as wind power penetration is still rather limited in most countries and power systems.

Wind power production introduces more uncertainty in operating a power system due to its variability and unpredictability. To meet this challenge, there will be a need for more flexibility in the power system. How much extra flexibility is needed depends on the one hand on how much wind power there is and on the other hand on how much flexibility there exists in the power system [4].

1.4. Wind Power Impacts on Power System

Wind power has impacts on power system reliability and efficiency. These impacts can be either positive or negative. Power system reliability relates to system security and adequacy. The system adequacy describes the amount of production and transmission capacity in varying load situations. The security of the power system is maintained by planning and operating the system in a way that minimises disturbances caused by faults. In order to manage disturbances, the system responsible grid operator assures that the system has enough reserves in power plants and in the transmission grid and keeps power transfers within the allowed limits [5].

Wind integration grid codes are required to ensure that wind farms do not adversely affect the power system with respect to security of supply, reliability of the grid and quality of the injected power. The following aspects are considered in the grid codes for the wind power integration:

- Active power and frequency control;
- Voltage control / Reactive power control;
- Power quality requirements;
- Fault ride-through (FRT);
- Low Voltage ride-through (LVRT).
- If the voltage drops more than 20% during faults, the Wind Farms without fault through capability may get disconnected. This worsens the critical grid situation.
- Even today, only few wind farms are able to fulfil the FRT capabilities.

Detailed requirements with respect to afore-mentioned aspects are stipulated in grid codes of various countries. When considering all of the above, and the fact that S.A. will be expanding its wind turbine fleet in the near future, a system that can emulate power system conditions in order to test integration issues of a wind generator in a laboratory environment can be beneficial for solving complex issues that are experienced in the industry. This is the motivation behind this thesis. It presents the development of a grid emulator system, which is capable of emulating several power quality conditions.

1.5. Literature Review of Grid Emulator

Installations of distributed renewable energy systems are increasing constantly, which leads to the decentralisation of energy generation and a dispersed grid. To ensure the power quality and stability, different grid codes for renewable energy systems are being defined in [6, 7, 8]. These grid codes stipulate the required response of renewable energy systems under different disturbances, such as voltage dips, unbalanced voltage, frequency variations and harmonic distortions. Renewable energy systems, such as wind turbines are being developed further in

order to comply with these standards and to act like a stable power plant and hence contribute to enhance the overall power quality [9].

The grid behaviour of the renewable energy systems is heavily influenced by the control techniques of these systems. These control techniques could be focused on the power electronic converter on generator side of the system or on the grid side. For further development of these control methods the conventional way is to simulate, test and prove the system performance on a scaled laboratory version of the system. The grid emulator discussed in this thesis has been developed to test such scaled renewable energy systems in the laboratory and to refine control methods associated with these systems.

A review of literature was conducted to analyse the grid behaviour when several devices are connected to a network. A grid simulator consisting of three single phase converters is discussed in [10], where PI-controllers are used in a synchronous reference frame to control the system performance. Another system is introduced in [11], which comprises two three-level voltage source converters connected by a three phase transformer to the load. Similarly, the control is implemented using PI controllers technique. However, two separate controllers for both positive and negative sequences components are used for unbalanced conditions.

In [12] a system is discussed with a series connected converter configuration for generating different types of voltage conditions rated up to a power of 30kVA and up to 1.5 times of the nominal voltage. This application is developed for medium voltage systems with state space control. It was shown that in order to implement all kinds of grid faults realistically, the dynamic response of the system should be fast. In [13] a step by step approach was adopted for LCL filter design. A mathematical model is presented which has a detailed comparison and analysis between L and LCL filter. Passive damping technique is also discussed for less complex industrial systems. A control strategy for integration of renewable energy sources to the distributed grid is presented in [14]. NPC VSI model is investigated during integration with AC grid. Fast dynamic response in tracking reactive power variations is also validated.

An FPGA algorithm is developed for three-level switching pattern in [15] which is further verified by modelling the simulation in Matlab/Simulink. In [16] a control strategy is presented

of vector control for the grid connected three-level NPC voltage source converter for high power DFIG drives. Both active and reactive power flow is studied in this paper with controlled DC link voltage.

Dual vector control under grid voltage dips analysed in [17, 18 and 19]. Stability is ensured for the whole system at every grid condition. Grid synchronisation was achieved by employing phase locked loop. Positive and negative sequence components are extracted using mathematical equations. Negative sequence was analysed to study the unbalance in the system. The synchronous reference frame *dq*- axis current controllers are used to manage the active and reactive power flow. Control was gained on each sequence component so as to generate all kind of voltage conditions and to mitigate those as well. Percentage unbalance in the output waveforms is also looked at in these references.

Different control techniques are proposed in this thesis to perform voltage dips, overvoltage and unbalanced voltage conditions and the back-to-back converter configuration is used to implement the grid emulator system. These converters can be used for low total harmonic distortion although they introduce high frequency distortion at high switching frequency. In order to remove these harmonic components, which are well above the fundamental grid frequency, two low pass filters are used, an L and an LCL filters. The LCL filter introduces resonances into the system, which leads to instability. The oscillations introduced by the LCL filter can be damped using different damping techniques which could be either active or passive. Passive damping is easier to implement compared to active damping because of its less complex control and no extra filtering components, although it introduces additional power dissipation due to the damping resistors.

For optimal performance of the converters, PI controllers played an important role. Controllers can be tuned using methods explained later. Inner control loops are tuned using the modulus optimum method and outer loops by using the symmetrical optimum method.

To handle power quality issues, especially in the case of unbalance, a sequence separation technique is implemented to analyse both positive and negative sequence components in the synchronous reference frame. Positive sequence gives information of the perfectly balanced

three phase conditions whereas the presence of negative sequence is indicative of an unbalance in the system. In order to control the unbalance a dual vector control is implemented.

1.6. Research Questions

The research presented in this thesis focuses on the full understanding and implementation, both in simulation and experimentally of a Grid Emulator System. All building blocks of the system are properly scrutinised. Special attention is given to optimising the control to produce different kinds of unbalanced grid conditions.

To achieve this, several research questions were proposed which include:

- How can a grid emulator be prototyped in the laboratory?
- Which system topologies exist for the development of grid emulator?
- How it can be controlled?
- What are the required grid codes?
- How can unbalance be generated with the system?
- What are the different filtering techniques?

1.7. Objectives

The objectives of the work carried out are to:

- Implement a grid emulator in the laboratory for the research project;
- Develop and implement the control of the grid emulator in simulations and experimentally using National Instrument PXI controller;
- Investigate and compare two converter topologies in terms of THD and dynamic response;
- Implement the grid emulator experimentally in the laboratory by combining the two converters in a back-to-back configuration;
- Identify and validate what is required from the grid emulator;
- Compare and estimate the performance of the converters.

1.8. Scope and Limitations

The system is designed for 30kW although the operating range was limited to 1kW due to restriction in hardware and time constraints. Only magnitude unbalance is implemented in this thesis. Harmonics and phase unbalance were therefore not considered due to the complex control and filtering requirements.

1.9. Contribution of the Thesis

This thesis presents the design, analysis and implementation of a grid emulator system. The system is capable of emulating several grid PQ disturbances, which include the following:

- Type A, B and E dips
- Symmetrical and non-symmetrical swells.

The system uses a two-level and a three-level VSI converter in a back-to-back configuration. The PWM switching signals and supervising control is implemented using NI PXI controller.

1.10. Structure

A literature review is presented in this chapter. In chapter 2 different power system quality issues are discussed, in order to highlight stability and instability conditions on a network. The grid emulator system's structure with detailed converter topologies is presented in chapter 3. Chapter 4 discusses the design of the LCL filter and different damping techniques. In chapter 5 control strategies are investigated and controller responses are analysed. The simulated system is developed and implemented in chapter 6. Chapter 7 explains the implementation of the system in the laboratory. The analysis of the results and comparisons between actual and expected results are presented in chapter 8. Conclusions and recommendations are finally presented in chapter 9.

CHAPTER 2

POWER SYSTEM QUALITY ISSUES

This chapter discusses the power quality issues in distributed generation systems. Power system stability is described in detail and thereafter the basic power quality problems which are to be implemented with the help of the grid emulator are discussed.

2.1. Power System Stability

Power system stability can be defined as the property of a power system that enables it to return to a state of equilibrium after being subjected to a disturbance. The operation is successful when it depends largely on the provision of consistent and continuous service. The power supply implies its firmness on its ideal accessibility, and therefore must be supplied with unvarying parameters of voltages and frequencies [20].

2.2. Requirements for Power System Stability

The success of operating a power system depends mainly on system stability. Ideally the load must be supplied with constant parameters for voltage, frequency and phase.

Studying the first necessity of power system stability is to observe that every consistent service needs to maintain the generators operation in step to each other, so as to make a sufficient capacity for the load. Voltage and current functions are disturbed and the transmission line can therefore trip. The separation of the generator from the system makes it asynchronous. Under normal conditions synchronous machines do not easily fall out of step [21].

Similarly, the second necessity of a reliable electric service is reliable power flow from generator to load. The power generating station and the consuming load centres are connected by a high-voltage transmission system. This generally needs a study of a huge physical area. A system will be considered more efficient, when total or maximum power will flow from generation to consumption [21].

2.3. Classification of Power System Stability

It is observed that the classification of the power system stability depends solely upon the condition of equilibrium between opposing forces. The mechanism of the system stability is formed through restoring forces, which will act whenever there are forces tending to speed up or speed down one or more machines with respect to the other. There is a state of equilibrium between the input mechanical torque and the output electrical torque of each machine and the speed remains constant under steady-state conditions. If the system disturbs this balance, the rotor of the generators will speed up or slow down [20].

A brief description of the types of power system stability is as follows:

- **Rotor Angle Stability**

  Rotor angle stability concerns with the synchronism of synchronous generators.

- **Frequency Stability**

  The system is considered frequency stable when the total generation output matches system load and loss demand.

- **Voltage Stability**

  Refers to the ability of a power system to maintain steady voltages at all buses in the system after being subjected to a disturbance from a given initial operating condition.

2.4. Power Quality Issues on the Network

The power system is routinely subjected to a variety of disturbances. Even the act of switching on of a household appliance can be regarded as a disturbance. However, given the size of the system and scale of perturbation that is caused by the switching on of an appliance in comparison to the size and capability of the interconnected system could be least influential towards power quality issues. Larger disturbances include lighting strikes, loss of transmission lines carrying bulk power due to overloading, or weather conditions like a tornado or ice stream, loss of generation of power from generating station, or the loss of major load. Any

disturbance in the system will cause the balance between the mechanical power input to the generator and electrical power output of the generator to be affected.

The power system is a completely non-linear system. Its dynamic performance can be enhanced with suitable control measurements having different response rates and features. The associated problems are affiliated with the performance of the interfaced system. In an isolated state the disturbance does not produce any change in power. If an unbalance is produced by variation in load, or by variation in generation of electrical power or by variation in network condition, a new working state is attained. In any case all interconnected synchronous machines should remain in step if the system is stable i.e. they should all remain working at the same speed. The system unbalance usually appears in the form of an oscillation. For a stable system, this oscillation will be damped and can be used further in the transmission lines carrying electrical energy. When a line connecting two groups of machines is tripped out by its control system, the two groups of machines would be disconnected. This problem is called the stability of the tie-line [20].

When the load is reduced, the current increases while the mechanical power that is being supplied to the synchronous machine is constant. The speed governor on each generating unit (in the case when there are more than one generator running parallel in the power system) will reduce the speed. In the case when load is increased while the power generation is decreased, some power supply lines will be disconnected. The stability problem is also mostly inclined by the strength of the transmission system with instability being the result of insufficient synchronising torque. The fault clearing time is slow, being in the order of 0.5 to 2.0 seconds or larger [20].

Power quality disturbances, which are to be implemented in this thesis are discussed below:

2.4.1. Voltage variation

This section deals with voltage quality problems associated with the grid that wind generators are exposed to. A wind farm can be connected to a low voltage, medium voltage and higher voltage networks. In the case of smaller installations, where a wind generator is connected to

weak electric grids such as medium voltage distribution networks (22kV), power quality problems may become a serious concern because of the close proximity of the generators to the loads. One of the power quality problems which pose a significant challenge is voltage dips. In developed countries it is known that from 75% up to 95% of the industrial sector is affected by the problems originated by this disturbance [22][23].

The voltage variation is directly related to active and reactive power variations. The voltage variation is commonly classified as following:

➢ Voltage Sag/Voltage Dips

Voltage dips are defined as the decrease of the defined voltage level from 10% to 90% at the normal power frequency, for durations of 0.5 cycles to 1 minute.

This problem is caused by faults on the transmission or distribution network. It also causes faults in the consumer's installation. Connection of heavy loads and start-up of large motors are also affected by voltage dip or voltage sag [22][23].

The outcomes of this problem are:

- malfunction of information technology equipment, namely microprocessor-based control;
- tripping of contactors and electromechanical relays;
- disconnection and loss of efficiency in electric rotating machines.

Voltage dips can be classified into symmetrical and non-symmetrical dips. A symmetrical dip occurs when all three phases sag without phase angle shifts. This type of a dip is classified as type A. Non symmetrical dips fall into two categories, single phase and double phase. The cause of each type of dip is a combination of either a phase-to-ground or phase-to-phase fault occurring in either a star or delta connected system. Figure 2.1 shows the dip classification. For the purpose of this thesis only the normal operating range will be considered. Type A, B and E dips are implemented with the help of a grid emulator.

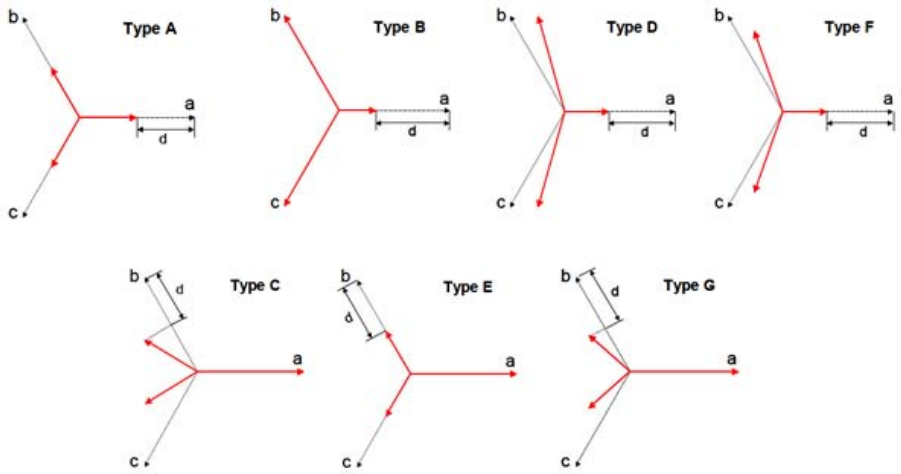


Figure 2.1: Voltage Dip Types [24]

➢ Voltage Swells

This is a momentary increase of the voltage at the power frequency outside the normal tolerances, with a duration of more than one cycle and typically less than a few seconds. This problem is caused by the start or stop of heavy loads, badly dimensioned power sources and badly regulated transformers mainly used during off-peak hours[22][23].

Some of the possible outcomes of voltage swells are:

- data loss,
- flickering of lighting and screens, stoppage or damage of sensitive equipment if the voltage values are too high.

➢ Short Interruptions

Short interruptions are the total interruption of electrical supply for the duration from a few milliseconds to one or two seconds. This is caused mainly due to the opening and automatic closure of protection devices to decommission a faulty section of the network. The main fault causes are insulation failure, lightning and insulator flashover [22][23]

Some of the possible outcomes of short interruptions are:

- tripping of protection devices;
- loss of information;
- malfunction of data processing equipment;
- Stoppage of sensitive equipment if they're not prepared to deal with this situation.

➢ Long duration voltage variation

Long duration voltage variation is the total interruption of electrical supply for a duration that is greater than one to two seconds. This is caused by equipment failure in the power system network, storms and objects (i.e. trees, cars) striking lines or poles, fire, human error and bad coordination or failure of a protection device [22][23].

The outcome of this problem is that all equipment stops working.

➢ Voltage fluctuation

Voltage fluctuation is the oscillation of voltage and the amplitude modulated by a signal with a frequency of 0 to 30 Hz. The magnitude of the voltage fluctuation depends on the grid strength, network impedance, phase angle and power factor of the system. This is caused by arc furnaces, frequent start/stop of electric motors and oscillating loads. The consequence of this problem is the flickering of lighting and tv-screens, giving the impression of unsteadiness of visual perception [23].

➢ Voltage spikes

Voltage spikes are very fast variations of the voltage value for durations from a few microseconds to a few milliseconds. These variations may reach thousands of volts, even in low voltage. It is caused by lightning, switching of lines or power factor correction capacitors and disconnection of heavy load. The consequences of this are destruction of components (particularly electronic components) and insulation materials, data processing errors or data loss and electromagnetic interference [23].

➢ Voltage unbalance

Voltage unbalance is a voltage variation in a three-phase system in which the three voltage magnitudes or the phase angle difference between them is not equal. This can be caused by large single-phase loads (induction furnaces, traction loads) and incorrect distribution of all single-phase loads by the three phases of the system (this may also be due to a fault)[23]. The consequence of voltage unbalance is unbalanced systems and that imply the existence of a negative sequence that is harmful to all three phase loads. Since many electrical devices are not designed to maintain their normal operation during a voltage dip, these disturbances are therefore a big problem. The behaviour of a wind turbine to a voltage dip is affected by the type of technology used. In the case of a fixed speed induction generator, a voltage dip initially decreases the active power supplied to the grid, while the reactive power consumed by the generator also decreases due to the demagnetisation of the machine. When the voltage recovers, the main effect is the absorption of reactive power in order to recover the magnetic flux. This extends the duration of the voltage dip and could be referred as low voltage ride through (LVRT) phenomena. The following figure 2.2 shows a typical voltage dip condition at the point of connection.

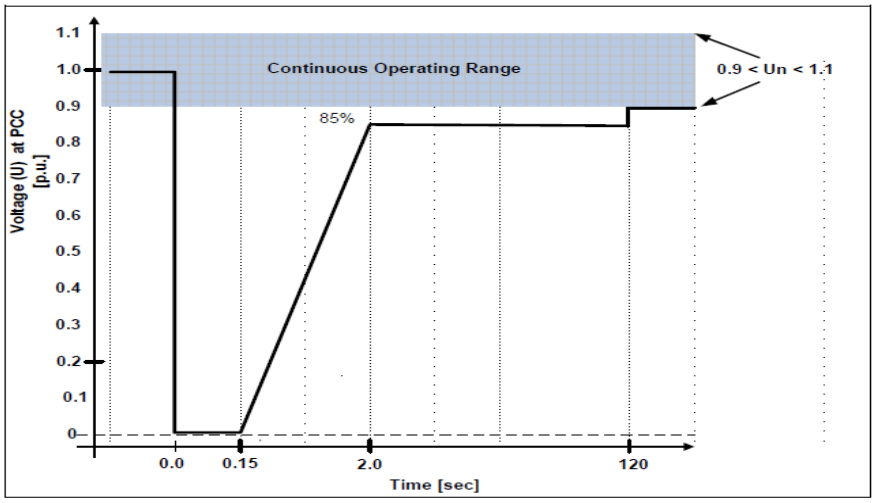


Figure 2.2: Instantaneous Voltage Dip Caused by a Fault [25]

2.4.2. Harmonics

Harmonics occur when voltage or current waveforms assume non-sinusoidal shapes. The waveforms correspond to the sum of different sine-waves with different magnitude and phases having frequencies that are multiples of the power system frequency [22].

This is caused by electric machines working above the knee of the magnetization curve, arc furnaces, welding machines, rectifiers, DC brush motors and non-linear loads, such as power electronics equipment, switched mode power supplies, data processing equipment and high efficiency lighting.

Consequences of harmonics are:

- increased probability in occurrence of resonance;
- neutral overload in 3-phase systems;
- overheating of all cables and equipment;
- loss of efficiency in electric machines;
- electromagnetic interference with communication systems;
- errors in measurements when using average reading meters;
- nuisance tripping of thermal protections.

2.4.3. Flicker

Voltage flicker describes dynamic variation in the network voltage caused by wind turbines or by varying loads. The power fluctuation from wind turbines occurs during continuous operation.

This is caused by fluctuation of active power and reactive power of wind turbine, arc furnace, arc lamps and capacitor switching [22].

The consequences of flicker are:

- degradation of power quality;
- damage to sensitive equipment.

2.4.4. Noise

The superimposing of high frequency signals on the waveform of the power-system frequency is called noise.

This is caused by electromagnetic interferences provoked by Hertzian waves, such as microwaves, television diffusion, and radiation due to welding machines, arc furnaces, and electronic equipment. Improper grounding may also be a probable cause [23].

Consequence of noise is:

- data loss and data processing errors.

2.5. Conclusion

This chapter introduced the necessary literature review on different power stability concerns. Understanding has been developed about the power quality issues in particular. This knowledge will be the base of implementing different unbalance voltage conditions with the aid of a grid emulator.

CHAPTER 3

GRID EMULATOR TOPOLOGY

This chapter describes the fundamental component of the grid emulator, i.e the configuration of converters. Both grid-side and load-side converters connected in back-to-back configuration play important role for the emulation of different voltage conditions and are therefore discussed in detail. The figure below shows the converters arrangement. A voltage source two-level and a NPC three-level converter were selected for the system control. The main theme was also to do the critical performance comparison between the two topologies. In this thesis both converters are tested in rectifier and inverter mode of operation by swapping their positions around as shown in the figure below. It shows two- and three-level converters connected between the grid to the load with the aid of an LCL filter and a DC link.

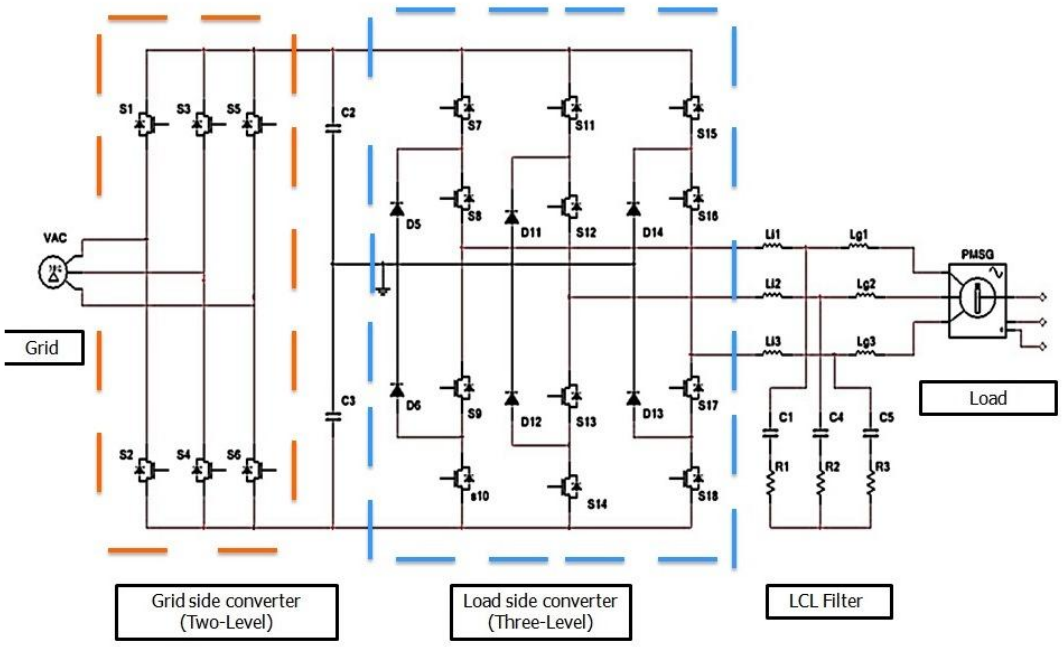


Figure 3.1 : Basic Configuration of Converters in a Grid Emulator

A voltage source converter in inversion mode (VSI) is mainly used to convert a fixed DC voltage into a three phase AC voltage with flexible magnitude and frequency. The output voltage could

be fixed or variable at a fixed or variable frequency. The output voltage waveforms of ideal inverters should be sinusoidal. However, the waveforms of practical inverters are not completely sinusoidal and contain certain harmonics which can be reduced significantly by switching techniques. The topology and component selection of an inverter plays an important role in the performance of the inverter. The conventional two-level inverter completely satisfies the low-voltage (L.V.) power applications where the nominal line-to-line 690 Vrms (IEC) 575 Vrms (ANSI). In contrast, the multilevel inverters offer significant advantages on the medium and high voltage applications. It produces a smoother output voltage with three voltage levels on each terminal and five on line-to-line. This voltage results in a lower THD.

3.1. Converter Topology:

Three phase converters are normally used for high-power applications. Two main topologies are considered during this thesis and are discussed below:

3.1.1. Two-Level converter:

This configuration comprises six switches (IGBT/diode). The diode actually provides a free-wheeling path for current. A pulse width modulation (PWM) will be applied for supervising control. The maximum potential impact on each switch can be equal to the DC link voltage, i.e E. The line-to-line voltage has three voltage levels (+E, 0, -E). Figure 3.2 shows a simplified circuit diagram of two-level converter connected to a load through an LCL filter. A detailed analysis is done of space vector modulation which is followed by switching time calculations with the help of PWM waveforms.

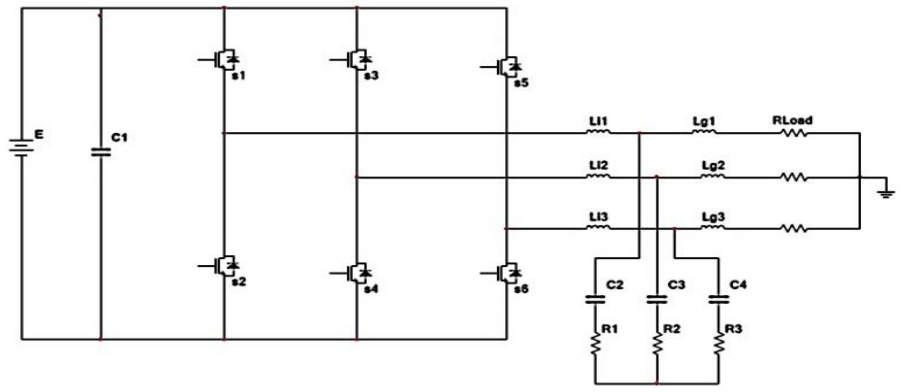


Figure 3.2: Two-Level Converter Circuit

3.1.2. Three-Level converter

In high power and high voltage applications, two-level converters have limitations in operating at high frequency mainly due to switching losses and constraints of device power ratings. Multilevel converters offer an alternate for medium and high voltage power applications. Three-level converters give a smoother output voltage with three voltage levels on each terminal and five between two lines and this results in lower THD. Switching losses are also reduced due to less commutation of the IGBTs per period as compared to the two-level converter. It also gives low dv/dt which is voltage variation per unit time and helps supplying lower harmonic content in the output voltage. Furthermore, dynamic voltage sharing capability results in extra benefit of multilevel topology. Multilevel converters have attracted tremendous interest in the power industry. They present a new set of features that are well suited for use in reactive power compensation. Increasing the number of voltage levels in the converter without requiring higher ratings for individual devices can increase the power rating. The unique structure of multilevel voltage source converters allows them to reach high voltages with low harmonic distortion, without the use of transformers or series connected synchronised switching devices. As the number of levels increase, the harmonic content of the output voltage waveform decreases significantly. Figure 3.3 shows a neutral point clamped (NPC) three-level converter connected to a DC-link. It has twelve switches (IGBT/Diode) and six clamping diodes which are actually fast reverse recovery diodes. The DC-link is distributed by two capacitor banks and its midpoint is connected to the load. The converter topology with modulation scheme and switching pattern is discussed further in this chapter.

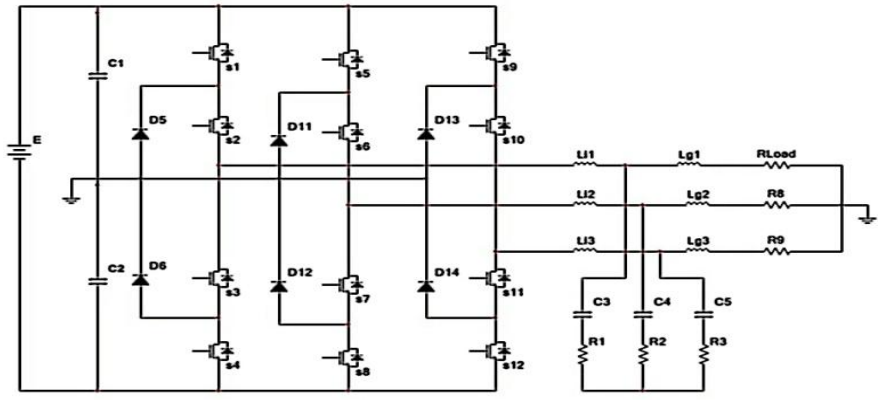


Figure 3.3: Neutral-Point-Clamped Three-Level Converter Circuit

The two converters discussed above are then connected in back-to-back configuration to form the grid emulator which interfaces the grid to the load. Voltage orientated control (VOC) is used to control both sides of the back-to-back converters. VOC is implemented in the synchronous reference frame and the relevant transformations are presented in the next sections.

3.2. Reference Frame Theory

Various reference frames exist where electrical space-phasor quantities can be represented. The synchronous reference frame is used to implement VOC and the transformations that lead to it are investigated in this section. Although voltage is referred to in the following examples, the methods can be applied to any space phasor quantity.

3.2.1. Natural reference frame

Voltages of a balanced three-phase system can be represented as phasors that have a length equal to their instantaneous magnitude with the phase difference of 120°. The resulting phasor has a magnitude of $1.5V_m$, where $V_m$is the peak value of the phase voltage, and rotates at a constant angular speed determined by the frequency of the phase voltages. The resultant line-to-line phasor is normalised to make it magnitude invariant. It will then have a magnitude that is in per unit, which is ideal for voltage control methods. The transformation is provided in equation 3.1.

$$v_s = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}) \tag{3.1}$$

3.2.2. Stationary reference frame

The stationary reference frame represents the phasor V_s on a set of orthogonal axes. The real axis α is chosen to be aligned with the phase A voltage phasor, whilst the imaginary β axis is in quadrature and leads by 90°. The transformation from the natural reference frame to the $\alpha\beta$ reference frame is called the Clarke transform and is presented in equation 3.2.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3.2)$$

3.2.3. Synchronous Reference Frame

The stationary reference frame components are time varying and sinusoidal in nature, for a balanced three phase system this complicates the controller design somewhat so the resultant phasor is rather projected onto a new set of axis that rotates at the same angular frequency (ω) as of the voltages. This new reference frame is called the synchronous or rotating reference frame. The real d-axis is chosen to correspond with the pole axis of the rotor in electrical machines and the grid current phasor in a grid-tied converter. The imaginary q-axis is in quadrature with the d-axis. The transformation from the $\alpha\beta$ reference frame to the *dq* reference frame is achieved with the Parke transform which is shown in equation 3.3.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (3.3)$$

3.3. Space Vector Modulation for Two-Level converter

Space vector modulation is the enhanced version of pulse width modulation and it is widely used to control real time applications, especially voltage source converters.

3.3.1. Space Vectors

Different switching states of a voltage source converter can be represented by space vectors. For two-level converters there are two switching states 'active' and 'zero'. In total, 2^3 space vector combinations are possible to control the converter. A typical hexagonal diagram having all the space vectors from $\vec{V}_0$ to $\vec{V}_7$ is shown in figure 3.4. $\vec{V}_1$ to $\vec{V}_6$ are active vectors whereas $\vec{V}_0$ & $\vec{V}_7$ are zero vectors. Zero vectors do not move in space therefore they are called stationary vectors. A reference vector $\vec{V}_{\text{ref}}$ rotates in space with angular displacement between α-axis and $\vec{V}_{\text{ref.}}$ When $\vec{V}_{\text{ref.}}$ completes one revolution in space, it corresponds to one cycle in time. The output voltage frequency of the converter can be maintained regulating the magnitude and angular speed of $\vec{V}_{\text{ref.}}$

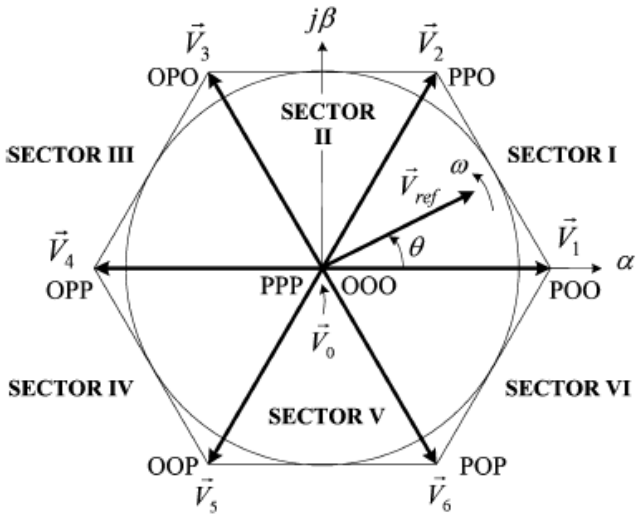


Figure 3.4: Space Vector Diagram for Two Level Converter[26]

3.3.2. Switching States

Space vectors shown in the figure above can be determined by permutations of the switching states of the VSC switches. As given in table 3.1 below, switching state 'P' indicates active state and upper switch in converter leg is on with positive terminal voltage while state 'O' indicates conduction of the lower switch which results in zero volts [26].

Table 3.1 Definition of switching states

Switching State	Leg *A*			Leg *B*			Leg *C*		
	S_1	S_4	V_{AN}	S_3	S_6	V_{BN}	S_5	S_2	V_{CN}
P	On	Off	V_d	On	Off	V_d	On	Off	V_d
O	Off	On	0	Off	On	0	Off	On	0

3.3.3. Dwell Time Calculations

The reference vector $\vec{V}_{ref}$ can be determined by applying magnitude of three stationary vectors in any given sector. During a sample time T_s this dwell time of each basic vector can be calculated as the duty cycle time. For example, if we consider $\vec{V}_{ref}$ in sector 1, It can be synthesized by the $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_0$ voltage vectors with T_a, T_b and T_o dwell times durations.

The dwell time for individual vector can be calculated with the help of Volt second equation given as:

$$\vec{V}_{ref} T_s = \vec{V}_1 T_a + \vec{V}_2 T_b + \vec{V}_0 T_o \tag{3.4}$$

$$T_s = T_a + T_b + T_o \tag{3.5}$$

The space vectors can also be defined as,

$$\vec{V}_{ref} = \left|\vec{V}_{ref}\right| e^{j\theta}, \qquad \vec{V}_1 = \frac{2}{3} V_d \ , \qquad \vec{V}_2 = \frac{2}{3} V_d e^{j\frac{\Pi 1}{3}} \qquad \text{and} \qquad \vec{V}_0 = 0$$

By combining the afore-mentioned equations and determining the real and imaginary components in α-β plane, we get

$$\mathrm{Re}: \left|\vec{V}_{ref}\right| (\cos\theta) T_s = \frac{2}{3} V_d T_a + \frac{1}{3} V_d T_b \tag{3.6}$$

$$\mathrm{Im}: \left|\vec{V}_{ref}\right| (\sin\theta) T_s = \frac{1}{\sqrt{3}} V_d T_b \tag{3.7}$$

The dwell times can be calculated by substituting for T_s from 3.5 and after solving 3.7 the dwell times can be expressed as

$$T_a = \frac{\sqrt{3} T_s \left|\vec{V}_{ref}\right|}{V_d} \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_b = \frac{\sqrt{3} T_s \left|\vec{V}_{ref}\right|}{V_d} \sin\theta$$

$$T_0 = T_s - T_a - T_b \tag{3.8}$$

The relation between $\vec{V}_{ref}$ and dwell times in sector 1 is summarised in the table below.

Table 3.2 : Vref location and Dwell Times

$\vec{V}$ *ref Location*	θ=0	0< θ < ∏/6	θ = ∏/6	∏/6< θ < ∏/3	θ=∏/3
Dwell Times	*Ta*>0 , *Tb*=0	*Ta >Tb*	*Ta= Tb*	*Ta< Tb*	*Ta =0, Tb>0*

If m_a is the modulation index, given as

$$m_a = \sqrt{3}\frac{\vec{V}_{ref}}{V_d}$$

Duration timing for switches in each sector is calculated as :

Table 3.3 : Duration time for each sector

Sector	Duration Times		
	Ta	Tb	To
1	$T_s m_a \sin\left(\frac{\Pi}{3}-\theta\right)$	$T_s m_a \sin(\theta)$	$T_s - T_a - T_b$
2	$T_s m_a \sin\left(\frac{2\Pi}{3}-\theta\right)$	$T_s m_a \sin\left(\theta-\frac{\Pi}{3}\right)$	$T_s - T_a - T_b$
3	$T_s m_a \sin(\Pi-\theta)$	$T_s m_a \sin\left(\theta-\frac{2\Pi}{3}\right)$	$T_s - T_a - T_b$
4	$T_s m_a \sin\left(\frac{4\Pi}{3}-\theta\right)$	$T_s m_a \sin(\theta-\Pi)$	$T_s - T_a - T_b$
5	$T_s m_a \sin\left(\frac{5\Pi}{3}-\theta\right)$	$T_s m_a \sin\left(\theta-\frac{4\Pi}{3}\right)$	$T_s - T_a - T_b$
6	$T_s m_a \sin(2\Pi-\theta)$	$T_s m_a \sin\left(\theta-\frac{5\Pi}{3}\right)$	$T_s - T_a - T_b$

3.3.4. Sequencing and Switching Time Calculation

There are seven switching states for each sector in a cycle. It always starts and ends with a zero state. This ensures there is no extra switching while shifting between sectors. As an example, in the case of sector 1 it starts with switching states 000-100-110-111-110-100-000. This whole time duration is Ts and each state cannot be greater than 1.

$$T_s = \frac{T_o}{4} + \frac{T_1}{2} + \frac{T_2}{2} + \frac{T_o}{2} + \frac{T_2}{2} + \frac{T_1}{2} + \frac{T_0}{4}$$

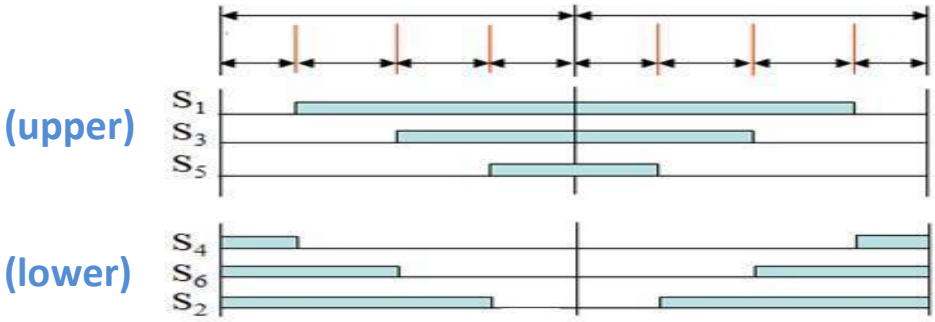
This has been calculated for all the sectors in the table given below.

Table 3.4 : Switching time for each sector

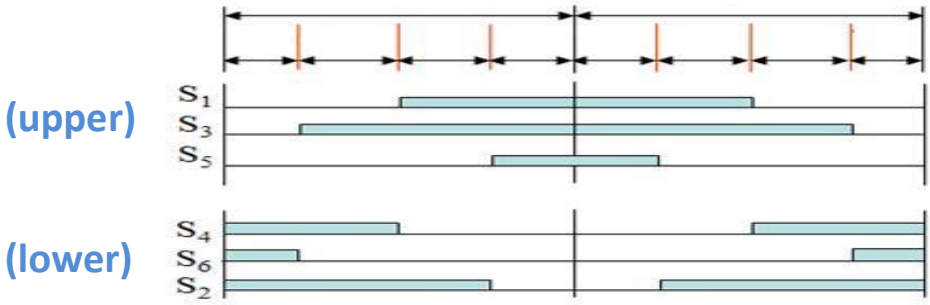
Switching Time Duration for Each Sector		
Sector No.	Upper Switches (S_1 S_3 S_5)	Lower Switches (S_4 S_6 S_2)
1	$T_{S1}=T_1+T_2+1/2T_0$ $T_{S3}=T_2+1/2T_0$ $T_{S5}=1/2T_0$	$T_{S4}=1/2T_0$ $T_{S6}=T_1+1/2T_0$ $T_{S2}= T_1+T_2+1/2T_0$
2	$T_{S1}=T_1+1/2T_0$ $T_{S3}=T_1+T_2+1/2T_0$ $T_{S5}=1/2T_0$	$T_{S4}=T_2+1/2T_0$ $T_{S6}=1/2T_0$ $T_{S2}= T_1+T_2+1/2T_0$
3	$T_{S1}=1/2T_0$ $T_{S3}=T_1+T_2+1/2T_0$ $T_{S5}=T_2+1/2T_0$	$T_{S4}=T_1+T_2+1/2T_0$ $T_{S6}=1/2T_0$ $T_{S2}= T_1+1/2T_0$
4	$T_{S1}=1/2T_0$ $T_{S3}=T_1+1/2T_0$ $T_{S5}=$ $T_1+T_2+1/2T_0$	$T_{S4}=T_1+T_2+1/2T_0$ $T_{S6}=T_2+1/2T_0$ $T_{S2}=1/2T_0$
5	$T_{S1}=T_2+1/2T_0$ $T_{S3}=1/2T_0$ $T_{S5}=T_1+T_2+1/2T_0$	$T_{S4}=T_1+1/2T_0$ $T_{S6}=T_1+T_2+1/2T_0$ $T_{S2}=1/2T_0$
6	$T_{S1}=T_1+T_2+1/2T_0$ $T_{S3}=1/2T_0$ $T_{S5}=T_1+1/2T_0$	$T_{S4}=1/2T_0$ $T_{S6}=T_1+T_2+1/2T_0$ $T_{S2}=T_2+1/2T_0$

Keeping in view the eight switching states the combination of the duty cycle states may result into the switching patterns that are quite adequate as shown in the Table 3.4. Figure 3.5 shows these switching patterns highlighted in Table 3.4 and are built in Multisim model to implement SVPWM. Waveforms showing sequences of all switching states for each sector are given below:

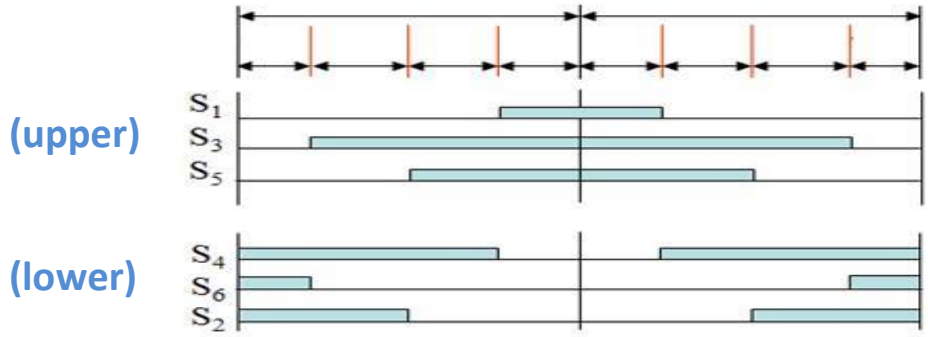
$1/4T_0$	$1/2T_1$	$1/2T_2$	$1/4T_0$	$1/4T_0$	$1/2T_1$	$1/2T_2$	$1/4T_0$



(Sector 1)



(Sector 2)



(Sector 3)

$1/4T_0$	$1/2T_1$	$1/2T_2$	$1/4T_0$	$1/4T_0$	$1/2T_1$	$1/2T_2$	$1/4T_0$

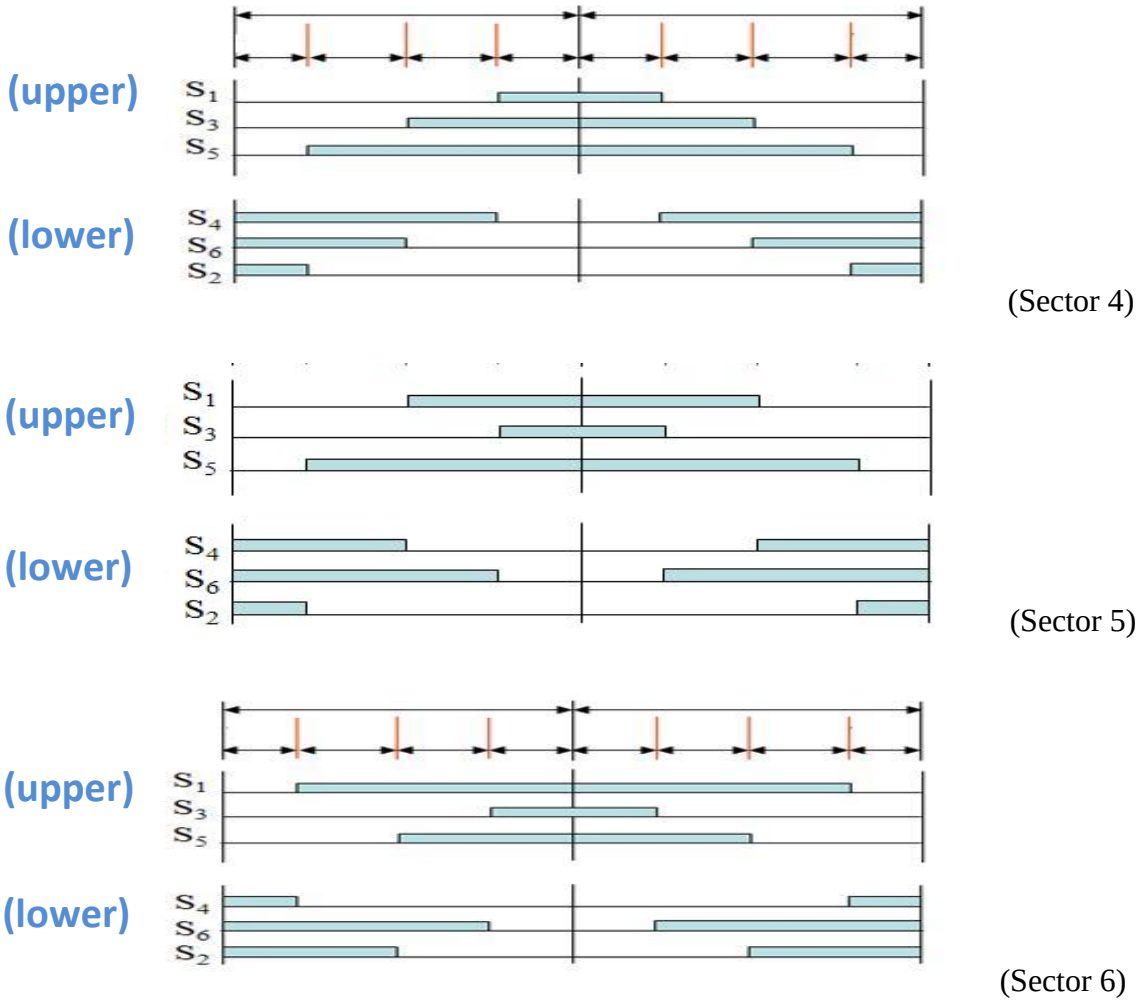


Figure 3.5 : Space Vector PWM Switching Patterns at Each Sector

3.4. Space Vector Modulation for Three-Level Converter

The space vector modulation scheme is discussed here for NPC Converter. Moreover, the commutation of switches is also explained.

3.4.1. Space Vectors

Different switching states can be represented by space vectors. For the three-level converter there are three switching states 'P' 'O' and 'N'. In total 3^3 space vector combinations are possible to control the converter. A typical hexagonal diagram showing all the space vectors from $\vec{V}_0$ to $\vec{V}_{18}$ and all the sectors from 1-6 are shown below in figure 3.6 and 3.7. $\vec{V}_1$ to $\vec{V}_6$ are small vectors which are formed by two switching states 'P' and 'N' having magnitude of $V_d/3$. The vector $\vec{V}_0$ is the zero vector representing three switching states 'PPP', 'NNN' and 'OOO'. Vectors $\vec{V}_7$ to $\vec{V}_{12}$ are medium vectors with magnitude $\sqrt{3}V_d$ /3 and $\vec{V}_{13}$ to $\vec{V}_{18}$ are large vectors with magnitude $2V_d/3$.

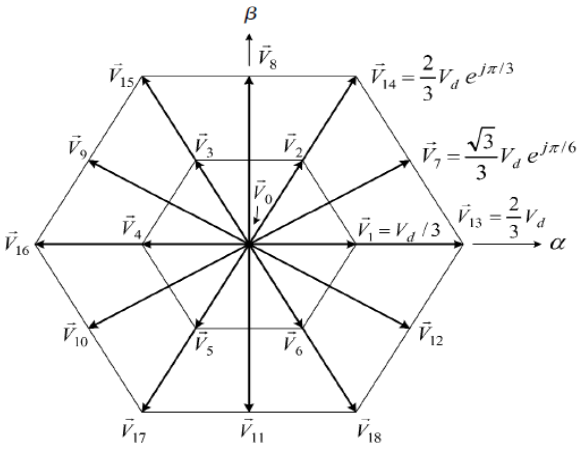


Figure 3.6 : Space Vector Diagram of the Three-Level NPC Converter[26]

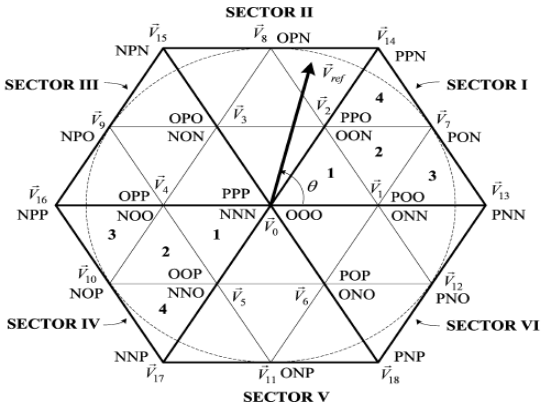


Figure 3.7 : Division of Regions and Sectors[26]

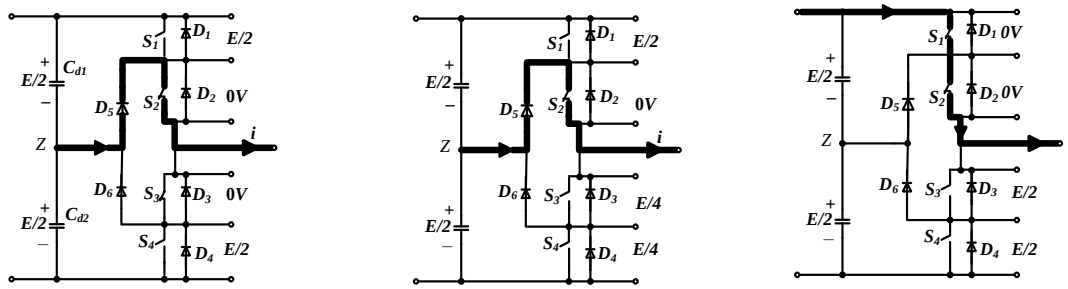
3.4.2. Switching States

The switching states of the NPC three-level converter are presented in the table given below. One leg of the converter has four switches. If these switches are divided into sets of two modules, then switching state 'P' corresponds to the top module being on and resulting in a terminal voltage of E/2 with respect to the neutral point. Similarly, switching state 'N' corresponds to the lower module being on and results in a terminal voltage –E/2. State 'O' corresponds to the inner two switches being on and the terminal voltage to be clamped to zero by means of the clamping diodes. Table 3.5 shows per phase switching sequence for the three-level converter.

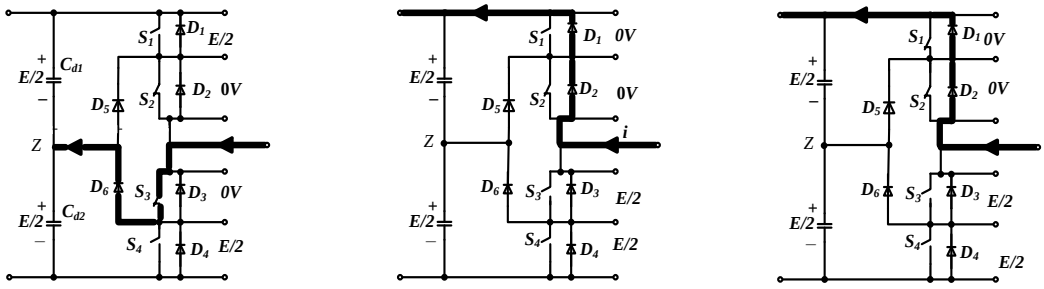
Table 3.5: Per phase switching sequence of three-level converter [26]

Switching State	Device Switching Status (Phase A)				Converter Terminal Voltage v_{AZ}
	S1	S2	S3	S4	
P	On	On	Off	Off	E/2
O	Off	On	On	Off	0
N	Off	Off	On	On	-E/2

The conduction of clamping diodes is dependent on the path of the load current through the converter. The transition of the switching state from 'O' to 'P' for positive and negative current flow is discussed below.



(a) Commutation with i >0



(b) Commutation with i <0

Figure 3.8: Commutation During a Transition from Switching State 'O' to 'P'.

As shown in the table 3.5 the switching state 'O' is achieved by turning switches S2 and S3 ON, state 'P' by turning S1 and S2 ON and 'N' state by turning S3 and S4 ON. The DC-link voltage is denoted as 'E' where C_{d1} and C_{d2} are the DC-link capacitors. Considering a state change from 'O' to 'P', for the case where i>0 , the switching state 'O' has switches S2 and S3 to an ON whilst S1 and S4 are OFF. The positive load current causes the clamping diode D5 into on-state. This results in voltages across switches S2 and S3 to be zero and the voltage on each switches S1 and S4 to be E/2. It can be seen that the current path during interval $\boldsymbol{\delta}$ remains the same as it was during 'O'. When switch S3 is fully turned off the voltage across S3 and S4 is E/4. The top switch S1 is then to achieve the switching state 'P'. The clamping diode D5 becomes reverse biased and turns off immediately. The load current is then commutated D5 to S1. The voltage across the two switches S3 and S4 is equally divided and becomes E/2 as both have already been in an off-state. The same procedure is applicable if current flows in a negative direction. It can be seen that half of the DC bus voltage is experienced by all the switches in the NPC converter during an excursion from state 'O' to 'P' for positive or negative current flow. Thus positive current flow in a single phase is achieved with two switches and a diode and negative current flow with two diodes and one switch.

3.4.3. Dwell Time Calculations

Any reference voltage space vector can be synthesized by applying adjacent basic vectors for a specific time. Unlike the two-level converter, here the sectors are further subdivided by into four triangular regions because of the additional switching states. A switching table for the three-level converter was developed by means of the analysis presented below.

During a sample time period T_s the dwell time can be calculated as a duty cycle time. As an example, lets consider $\vec{V}_{ref}$ located in region 2 of sector 1 as shown in figure 3.9. It can be synthesized with $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_7$ basic voltage vectors applied for specific dwell times T_a, T_b and T_c. The dwell times can be calculated by the means of volt second balancing equation.

$$\vec{V}_{ref}T_s = \vec{V}_1T_a + \vec{V}_7T_b + \vec{V}_2T_c \tag{3.9}$$

Where,

$$T_s = T_a + T_b + T_c \tag{3.10}$$

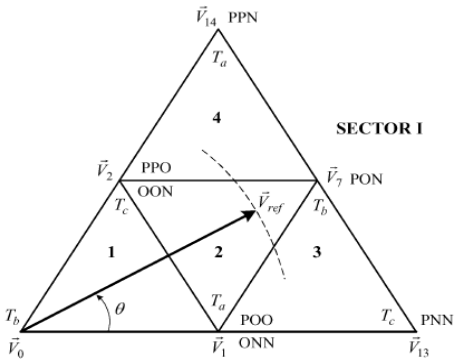


Figure 3.9: Voltage Reference Vector in Region 2 of Sector I [25]

With reference to the figure 3.9 the voltage space vectors can be expressed as, where V_d is the terminal voltage

$$\vec{V}_1 = \frac{1}{3}V_d \quad , \quad \vec{V}_2 = \frac{1}{3}V_d e^{j\frac{\pi}{3}} \quad , \quad \vec{V}_7 = \frac{\sqrt{3}}{3}V_d e^{j\frac{\pi}{6}} \quad , \quad \vec{V}_{ref} = \left|\vec{V}_{ref}\right| e^{j\theta}$$

By substituting the above expressions into 3.10 the following equation can be written as:

$$\frac{1}{3}V_d T_a + \frac{\sqrt{3}}{3}V_d e^{j\frac{\pi}{6}} T_b + \frac{1}{3}V_d e^{j\frac{\pi}{3}} T_c = \left|\vec{V}_{ref}\right| e^{j\theta} T_s \tag{3.11}$$

By expanding the polar form of the vector operators into rectangular form the following can be written,

$$\begin{aligned} &\frac{1}{3}V_d T_a + \frac{\sqrt{3}}{3}V_d (\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}) T_b + \frac{1}{3}V_d (\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}) T_c \\ &= \left|\vec{V}_{ref}\right| (\cos\theta + j\sin\theta) T_s \end{aligned} \tag{3.12}$$

By separating the real and imaginary parts of equation 3.12, the following expressions can be written:

$$\mathrm{Re}: T_a + \frac{3}{2}T_b + \frac{1}{2}T_c = 3\frac{\left|\vec{V}_{ref}\right|}{V_d}(\cos\theta) T_s$$

$$\text{Im}: \frac{\sqrt{3}}{2} T_b + \frac{\sqrt{3}}{2} T_c = 3 \frac{\left| \vec{V}_{ref} \right|}{V_d} (\sin\theta) T_s \qquad (3.13)$$

Solving time expressions

$$T_a = T_s[1 - 2m_a \sin\theta]$$

$$T_b = T_s[2m_a \sin(\theta + \frac{\pi}{3}) - 1] \qquad \text{for } \leq \theta < \frac{\pi}{3}$$

$$T_c = T_s[1 - 2m_a \sin(\frac{\pi}{3} - \theta)] \qquad (3.14)$$

Where m_a is the modulation index, given as

$$m_a = \sqrt{3} \frac{\vec{V}_{ref}}{V_d}$$

A Similar approach can be used to calculate the dwell times for $\vec{V}_{\text{ref}}$ located in other regions of sector I. The expressions for the dwell times of $\vec{V}_{\text{ref}}$ in sector 1 is shown in table 3.6 below .

Table 3.6 : Dwell time calculation for $\vec{V}_{ref}$ in Sector-1 [26]

Region	*Ta*		*Tb*		*Tc*	
1	V_1	$T_s.\left\lfloor 2m_a.\sin.\left(\frac{\Pi}{3} - \theta\right)\right\rfloor$	V_0	$T_s.\left\lfloor 1 - 2m_a.\sin.\left(\theta + \frac{\Pi}{3}\right)\right\rfloor$	V_2	$T_s.[2m_a.\sin\theta]$
2	V_1	$T_s.\lfloor 1 - 2m_a.\sin.(\theta)\rfloor$	V_7	$T_s.\left\lfloor 2m_a.\sin.\left(\theta + \frac{\Pi}{3}\right) - 1\right\rfloor$	V_2	$T_s.\left\lfloor 1 - 2m_a.\sin.\left(\frac{\Pi}{3} - \theta\right)\right\rfloor$
3	V_1	$T_s.\left\lfloor 2 - 2m_a.\sin.\left(\theta + \frac{\Pi}{3}\right)\right\rfloor$	V_7	$T_s.[2m_a.\sin\theta]$	V_{13}	$T_s.\left\lfloor 2m_a.\sin.\left(\frac{\Pi}{3} - \theta\right) - 1\right\rfloor$
4	V_{14}	$T_s.[2m_a.\sin\theta - 1]$	V_7	$T_s.\left\lfloor 2m_a.\sin.\left(\frac{\Pi}{3} - \theta\right)\right\rfloor$	V_2	$T_s.\left\lfloor 2 - 2m_a.\sin.\left(\theta + \frac{\Pi}{3}\right)\right\rfloor$

Similarly the dwell times for other sectors can be calculated by using equations 3.9-3.14. Each dwell time expression in table 3.6 has complex sine notations for duty cycle calculations. Now if this concept is adapted into FPGA code, these expressions would consume a lot of memory which is not an efficient way. Instead of this, these times can be transformed in three phase voltage expressions as shown in the following equations.

If, $$V_a = \sin\theta \tag{3.15}$$

Then $$V_b = \sin(\theta + \frac{2\Pi}{3})$$

$$= \sin(\theta).\cos(\frac{2\Pi}{3}) + \cos(\theta).\sin(\frac{2\Pi}{3}) \quad = \sin(\theta).(-\frac{1}{2}) + \cos(\theta).(\frac{\sqrt{3}}{2})$$

Therefore, V_b can also be written as:

$$V_b = \sin(\frac{\Pi}{3} - \theta) \tag{3.16}$$

Similarly, $$V_c = \sin(\theta + \frac{4\Pi}{3})$$

$$= \sin(\theta).\cos(\frac{4\Pi}{3}) + \cos(\theta).\sin(\frac{4\Pi}{3}) \quad = \sin(\theta).(-\frac{1}{2}) + \cos(\theta).(-\frac{\sqrt{3}}{2})$$

and V_c can also be written as

$$V_c = -\sin(\theta + \frac{\Pi}{3}) \tag{3.17}$$

Similarly, $$-V_a = -\sin\theta \tag{3.18}$$

$$-V_b = \sin(\theta - \frac{\Pi}{3}) \tag{3.19}$$

And $$-V_c = \sin(\theta + \frac{\Pi}{3}) \quad (3.20)$$

3.4.4. Sector and Region Selection

The sector can be selected with the help of following equation:

$$SectorNumber = A + 2B + 4C \quad (3.21)$$

Where, $$A = \begin{Bmatrix} 1, V_a > 0 \\ 0, V_a < 0 \end{Bmatrix}, \quad B = \begin{Bmatrix} 1, V_b > 0 \\ 0, V_b < 0 \end{Bmatrix}, \quad C = \begin{Bmatrix} 1, V_c > 0 \\ 0, V_c < 0 \end{Bmatrix}$$

The regions selection can be done in accordance with the flowchart shown in figure 3.10:

If, $V_\alpha + \frac{\sqrt{3}}{3} V_\beta - \frac{V_{DC}}{3} < 0$ the $\vec{V}_{ref}$ is in region 1 and if not, the vector could be in region 2.

Then if, $V_\alpha - \frac{\sqrt{3}}{3} V_\beta - \frac{V_{DC}}{3} > 0$ then the vector is in region 2 else it could be in region 3.

Then if $V_\alpha - \frac{\sqrt{3}}{6} V_{DC} < 0$ then the vector is in region 3 else in region 4.

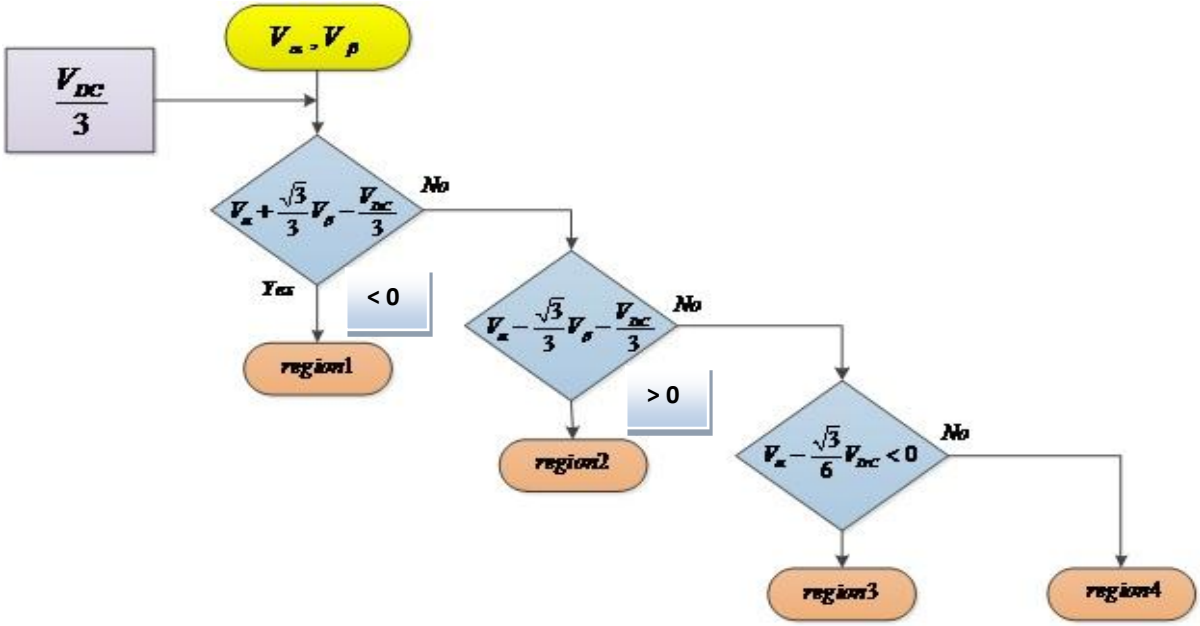


Figure 3.10: Region Selection Flowchart

3.4.5. Sequencing and Switching Time Calculation

The timing of each switch is dependent on the sector and region that $\vec{V}_{ref}$ is located in. Since each sector has four regions this means that there will be: 4switches * 3phases* 6sectors* 4 regions= 288 permutations of the converter output. However, the upper and lower set of switches of a leg works in a complementary manner, so only 144 permutations has to be calculated. By using equations 3.15-3.20, simplified expressions for the dwell times Ta, Tb and Tc for each sector and region are presented in the table below:

Table 3.7: Dwell time calculations in terms of Va, Vb & Vc

Sector	Time	Region 1	Region 2	Region 3	Region 4
1	T_a T_b T_c	$T_s\left[2m_aV_b\right]$ $T_s\left[1+2m_aV_c\right]$ $T_s\left[2m_aV_a\right]$	$T_s\left[1-2m_aV_a\right]$ $-T_s\left[2m_aV_c-1\right]$ $T_s\left[1-2m_aV_b\right]$	$T_s\left[2+2m_aV_b\right]$ $T_s\left[2m_aV_a\right]$ $T_s\left[2m_aV_b-1\right]$	$T_s\left[2m_aV_a-1\right]$ $T_s\left[2m_aV_b\right]$ $T_s\left[2+2m_aV_c\right]$
2	T_a T_b T_c	$T_s\left[2m_aV_b\right]$ $T_s\left[1+2m_aV_c\right]$ $T_s\left[2m_aV_a\right]$	$-T_s\left[2m_aV_c-1\right]$ $T_s\left[2m_aV_b\right]$ $T_s 2m_a\left[1-V_a\right]$	$T_s\left[1+2m_aV_c\right]$ $T_s\left[2m_aV_a-1\right]$ $T_s\left[2m_aV_b+1\right]$	$T_s\left[1-2m_aV_a\right]$ $-T_s\left[2m_aV_c\right]$ $-T_s\left[2m_aV_b-1\right]$
3	T_a T_b T_c	$T_s\left[2m_aV_a\right]$ $T_s\left[1+2m_aV_b\right]$ $T_s\left[2m_aV_c\right]$	$T_s\left[1+2m_aV_b\right]$ $T_s\left[2m_aV_c\right]$ $-T_s\left[2m_aV_a-1\right]$	$-T_s\left[2m_aV_c+1\right]$ $-T_s\left[1+2m_aV_b\right]$ $T_s\left[1-2m_aV_a\right]$	$-T_s\left[1-2m_aV_a\right]$ $-T_s\left[2m_aV_c\right]$ $-T_s\left[2m_aV_c-1\right]$
4	T_a T_b T_c	$-T_s\left[2m_aV_a\right]$ $T_s\left[1-2m_aV_c\right]$ $-T_s\left[2m_aV_b\right]$	$-T_s\left[2m_aV_b-1\right]$ $-T_s\left[2m_aV_a\right]$ $T_s 2m_a\left[1-V_c\right]$	$T_s\left[2m_aV_b-1\right]$ $-T_s\left[1-2m_aV_c\right]$ $T_s\left[1+2m_aV_a\right]$	$T_s\left[1-2m_aV_c\right]$ $T_s\left[2m_aV_b\right]$ $T_s\left[1+2m_aV_b\right]$
5	T_a T_b T_c	$T_s\left[2m_aV_c\right]$ $T_s\left[1+2m_aV_a\right]$ $T_s\left[2m_aV_b\right]$	$T_s\left[1+2m_aV_a\right]$ $T_s\left[2m_aV_b\right]$ $T_s\left[2m_aV_c+1\right]$	$-T_s\left[2m_aV_b+1\right]$ $-T_s\left[2m_aV_a+1\right]$ $-T_s\left[2m_aV_c+1\right]$	$T_s\left[2m_aV_b-1\right]$ $-T_s\left[2m_aV_c\right]$ $T_s\left[1+2m_aV_a\right]$
6	T_a T_b T_c	$-T_s\left[2m_aV_c\right]$ $-T_s\left[1+2m_aV_b\right]$ $-T_s\left[2m_aV_a\right]$	$-T_s\left[1+2m_aV_a\right]$ $-T_s\left[2m_aV_c\right]$ $-T_s\left[2m_aV_b+1\right]$	$T_s\left[2m_aV_a+1\right]$ $T_s\left[1+2m_aV_c\right]$ $T_s\left[2m_aV_b-1\right]$	$T_s\left[1-2m_aV_b\right]$ $-T_s\left[2m_aV_a\right]$ $T_s\left[2m_aV_c-1\right]$

The switching states for all the regions in sector-1 are shown in figure 3.11. Sequencing of waveforms for switch time calculation in sector-1 for all four regions is given as :

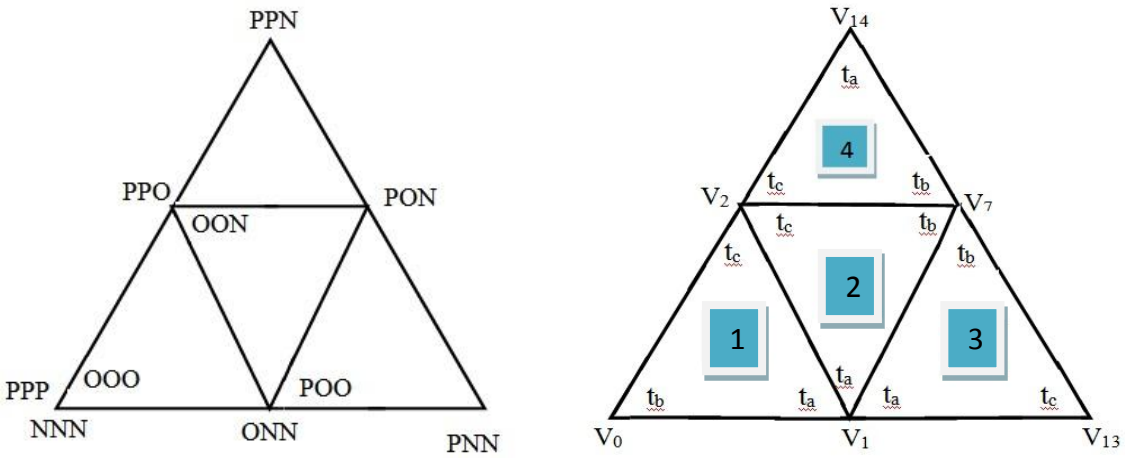
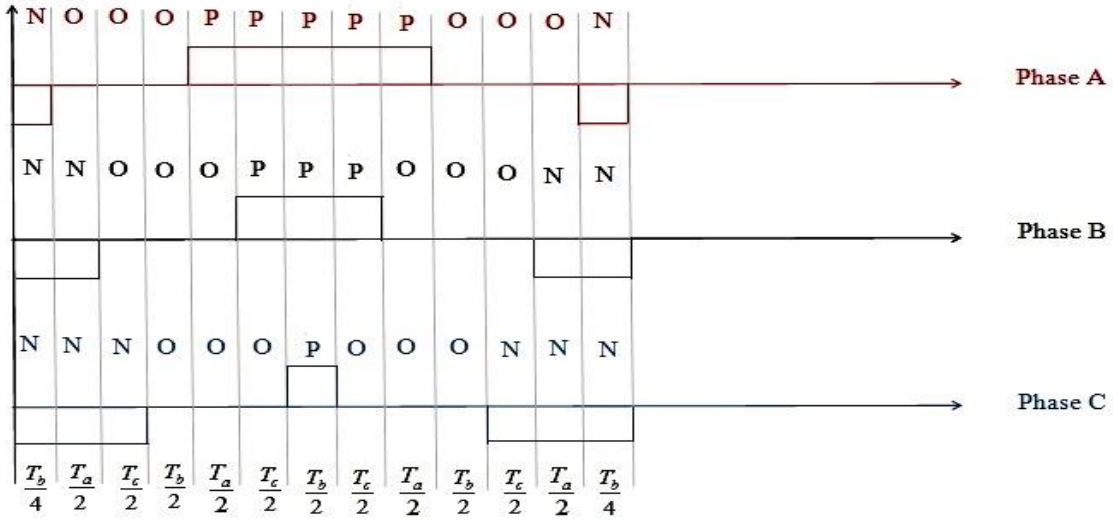


Figure 3.11: Space Vector Diagram of Sector 1 with All Four Regions

Region 1:

Regulation of phases and corresponding switching states are shown below. Waveforms show the switch on times for each leg of the converter.

A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
N	N	N	O	N	N	O	O	N	O	O	O	P	O	O	P	P	O	P	P	P	P	P	O	P	O	O	O	O	O	O	O	N	O	N	N	N	N	N



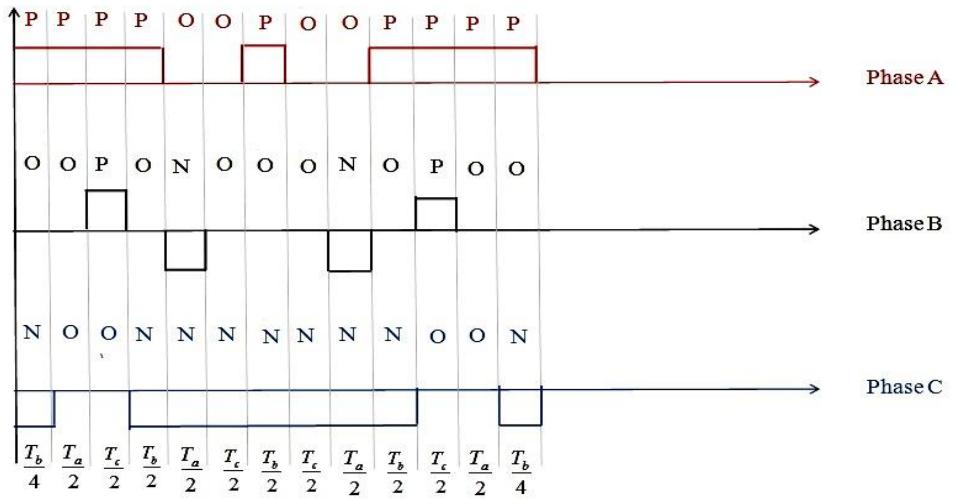
With reference to the definitions in Figure 3.8, timing expressions are calculated only for switch 1 and 2 since switch 3 and 4 are complementary functions of T1 and T2 and need not to be calculated. Dwell timings for one period are synthesized by calculating the full switching time divided by 2:

$S_{1A}: \frac{T_a}{2}+\frac{T_c}{2}+\frac{T_b}{4}$ $S_{1B}: \frac{T_c}{2}+\frac{T_b}{4}$ $S_{1C}: \frac{T_b}{4}$

$S_{2A}: \frac{T_b}{4}$ $S_{2B}: \frac{T_b}{4}+\frac{T_a}{2}$ $S_{2C}: \frac{T_a}{2}+\frac{T_c}{2}+\frac{T_b}{4}$

Region 2:

A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
P	O	N	P	O	O	P	P	O	P	O	N	O	N	N	O	O	N	P	O	N	O	O	N	O	N	N	P	O	N	P	P	O	P	O	O	P	O	N

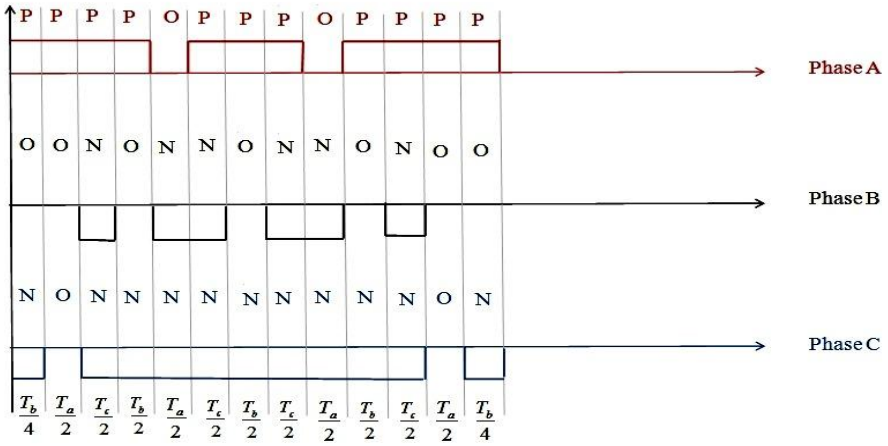


$S_{1A}: \frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$ $S_{1B}: \frac{T_c}{2}$ $S_{1C}: 0$

$S_{2A}: 0$ $S_{2B}: \frac{T_a}{2}$ $S_{2C}: \frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$

Region 3:

A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
P	O	N	P	O	O	P	N	N	P	O	N	O	N	N	P	N	N	P	O	N	P	N	N	O	N	N	P	O	N	P	N	N	P	O	O	P	O	N

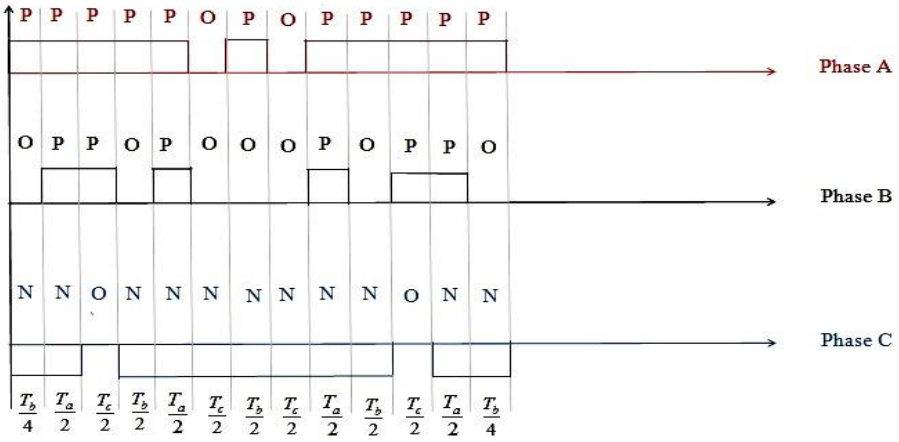


$S_{1A}: \frac{T_a}{2}+T_b+T_c$ S_{1B}: 0 S_{1C}: 0

S_{2A}: 0 $S_{2B}: \frac{T_a}{2}+T_c$ $S_{2C}: \frac{T_a}{2}+T_b+T_c$

Region 4:

A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
P	O	N	P	P	N	P	P	O	P	O	N	P	P	N	O	O	N	P	O	N	O	O	N	P	P	N	P	O	N	P	P	O	P	P	N	P	O	N



S_{2A}: 0 S_{2B}: 0 $S_{2C}: T_a+T_b+\frac{T_c}{2}$

$S_{1A}: T_a+T_b+\frac{T_c}{2}$ $S_{1B}: T_a+\frac{T_c}{2}$ S_{1C}: 0

The expressions calculated above for sector-1 can be tabulated as:

Table 3.8: Dwell Time Calculation for Sector-1

Region / Time	1	2	3	4
S1A	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+T_c$	$T_a+T_b+\frac{T_c}{2}$
S2A	$\frac{T_b}{4}$	0	0	0
S1B	$\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_c}{2}$	0	$T_a+\frac{T_c}{2}$
S2B	$\frac{T_b}{4}+\frac{T_a}{2}$	$\frac{T_a}{2}$	$\frac{T_a}{2}+T_c$	0
S1C	$\frac{T_b}{4}$	0	0	0
S2C	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+T_c$	$T_a+T_b+\frac{T_c}{2}$

Dwell time calculation for sector-1 is presented in this chapter and a full table for the other five sectors is given in Appendix-A.

3.5. Conclusion

This chapter presented an overview of the two-level and three-level converter topologies and detailed expressions for the switching time calculations. Dwell timings for the reference vector are derived with the help of equations and PWM waveforms. The switching time calculation for the three-level converter was shown to be extensive in comparison with the two-level topology. A sophisticated and powerful control system would therefore be required to implement these algorithms.

CHAPTER 4

FILTER & DC-link DESIGN

This chapter outlines techniques for the design of an LCL filter. Several methods are discussed for damping resonance introduced by the filter. The filter is mathematically modelled and appropriate component values are chosen. Different active damping techniques have been discussed and for each of them frequency response is studied. The theory that was developed in the previous chapters is then applied to the design of the filter and the DC link for the system.

4.1. Introduction

Systems which are in the presence of power electronic converters experience current harmonics in the system. A large inductance can be connected but this will bring poor dynamics and operating range. Simple 'L' filters have been used in the past to get rid of these harmonics and ripples. They can be considered as good options for low power systems where with low inductance values acceptable amount of current harmonic attenuation is achieved. Moreover, there are very few design options to consider, which makes them easy to implement in a system. However, as the power of the system increases, the inductance value increases and hence the inductor becomes larger and more expensive. Under these conditions it is feasible to use an LCL filter to reduce the cost and size of the system. A higher order LCL filter can be used to get rid of current ripples using small inductance values. With high switching frequency, switches in the converter introduce high current distortions. At higher frequencies an LCL filter has a larger current harmonic attenuation for the same value of inductance used in an L-filter. This technique can be considered ideal to achieve maximum attenuation with small inductance values. However, while designing an LCL filter extra characteristics must be taken into account such as ripple current, resonance, filter size and the reactive power absorbed [27][28][29].

4.2. Transfer function of the LCL filter

The transfer function of an LCL filter can be calculated by considering figure 4.1. Expressions for a single phase will be obtained as the remaining two phases are identical to it [34].

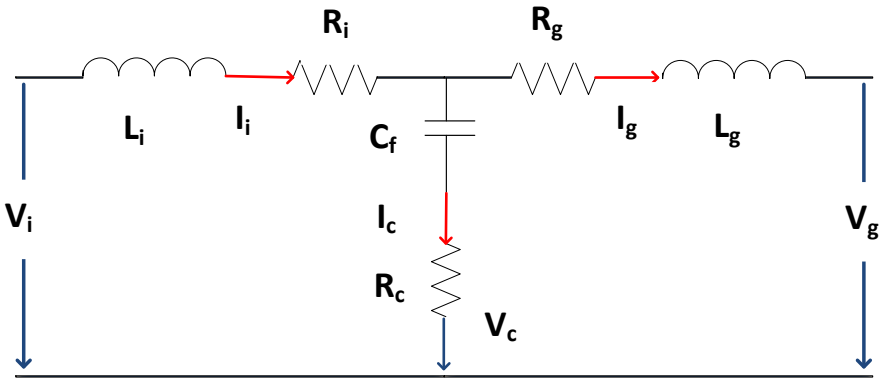


Figure 4.1: LCL Filter Equivalent Circuit

Applying Kirchoff's Law , the filter can be modelled by the following equations :

$$I_i - I_c - I_g = 0 \tag{4.1}$$

$$V_i - V_c = I_i(sL_i + R_i) \tag{4.2}$$

$$V_c - V_g = I_g(sL_g + R_g) \tag{4.3}$$

$$V_c = I_c\left(\frac{1}{sC_f} + R_c\right) \tag{4.4}$$

Where,

- V_i is the inverter voltage
- I_i is the inverter current
- V_c is the voltage drop across filter capacitance
- I_c is the current through filter capacitance

- V_g is the grid voltage
- I_g is the grid current
- L_i is the filter inductance on inverter side
- R_i is the inverter side parasitic resistance
- C_f is the filter capacitance
- R_c is the parasitic resistance of the capacitor
- L_g is the filter inductance on grid side
- R_g is the grid side parasitic resistance

An LCL filter can be represented by the block diagram in figure 4.2, using equations 4.1-4.4:

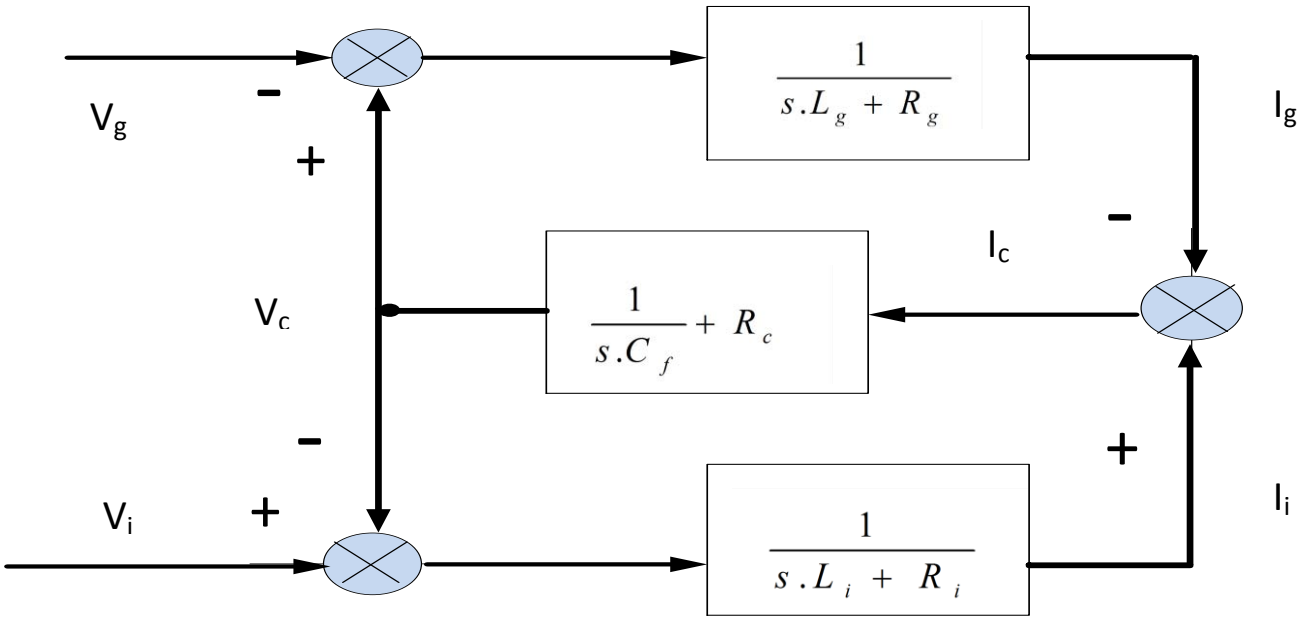


Figure 4.2: Block Diagram of an LCL Filter

Hence the transfer function can be written as:

$$H_{LCL} = \frac{I_g}{V_i} \tag{4.5}$$

To determine the complete transfer function, the grid voltage is assumed to be an ideal voltage source where the effects of the grid are ignored. From the equations 4.3 and 4.4 the following expressions are obtained:

$$I_g(sL_g + R_g) = I_c(\frac{1}{sC_f} + R_c) \tag{4.6}$$

$$I_c = I_g \frac{s^2 C_f L_g + sC_f R_g}{sC_f R_c + 1} \tag{4.7}$$

Equation 4.2 can also be written as:

$$V_i = V_c + I_i(sL_i + R_i) \tag{4.8}$$

The complete transfer function of an LCL filter is represented by :

$$H_{LCL} = \frac{sR_cC_f + 1}{s^3 L_g L_i C_f + s^2 C_f (L_g(R_c + R_i)) + s(L_g + L_i + C_f(R_cR_g + R_cR_i + R_gR_i)) + R_gR_i} \tag{4.9}$$

A simplified expression can be achieved by ignoring the parasitic resistances

$$H_{LCL} = \frac{1}{s^3 L_g L_i C_f + s(L_g + L_i)} \tag{4.10}$$

Figure 4.3 shows the bode plots of an L and LCL filter with an identical total inductance.

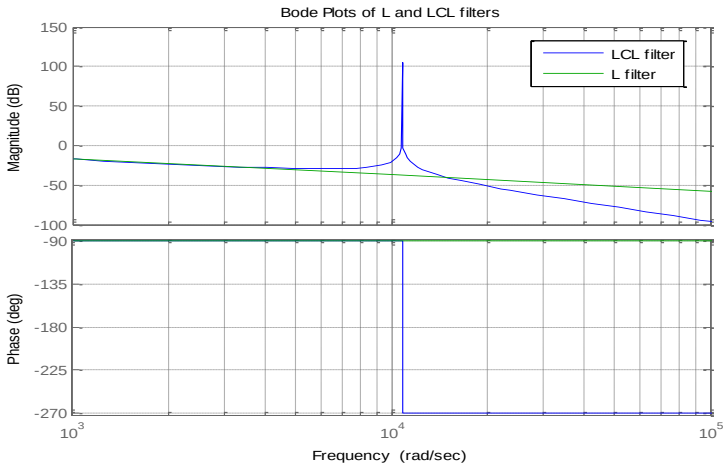


Figure 4.3: L and LCL Filter Bode Plots

Figure 4.3 indicates that for the same inductance, the LCL filter achieves greater attenuation at high frequencies but introduces a resonance in to the system which can lead to instability if not damped sufficiently.

4.3. Damping Techniques

To increase the system stability the resonance caused by an LCL filter should be damped. Two types of damping techniques exist namely passive and active damping. An active damping technique incurs no power losses but introduces control complexity. Passive damping is simple to implement but power is lost through additional passive components.

4.3.1. Passive Damping

Passive damping is shown in figure 4.4. A resistor is introduced either in series or parallel to the filter inductor or capacitor. The presence of the resistor damps the oscillations caused by the filter resonance.

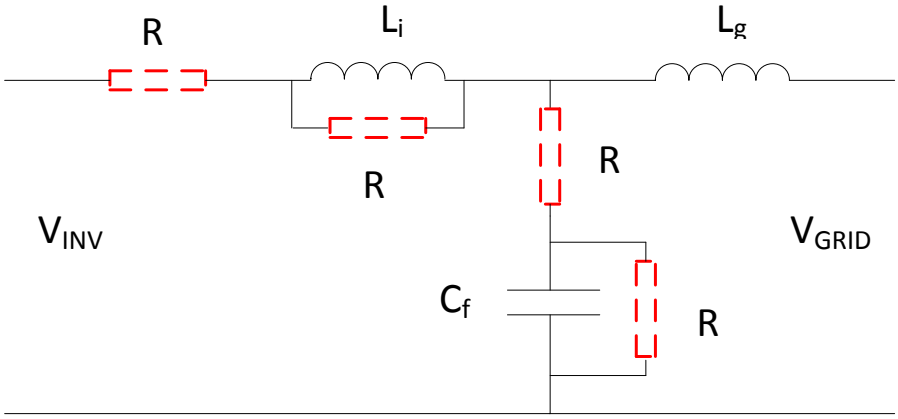


Figure 4.4: Passive Damping Resistor Positions

The most common configuration is the resistor either in series or in parallel with the filter capacitor. Simple band stop filters with a resistor in series are sometimes proposed, either in the phase or in the neutral. A series filter is intended to block harmonic currents rather than provide a controlled path for it so that there is a large harmonic voltage drop across it. This harmonic voltage appears across the supply on the load side. Since the supply voltage is heavily distorted, it is no longer within the standards for which equipment was designed and warranted. Some equipment is relatively insensitive to this distortion, but some are very

sensitive. Series filters can be useful in certain circumstances, but should be carefully applied as they cannot be recommended as a general purpose solution.

A damping resistor which is in series with the capacitor, results in more stability. Total power loss can be calculated through the addition of the damping resistors as given in equation 4.11.

$$P_{series} = 3R\sum_{h}[I_i(h) - I_g(h)]^2 \tag{4.11}$$

Where $I_i(h)$ and $I_g(h)$ are the order *h* harmonics of the inverter and grid side currents. In the case when a resistor is connected in parallel with the filter capacitor, power losses are acquired from equation 4.12 where $V_c(h)$ is the order *h* capacitor voltage. The power loss decreases as the damping resistance increases. This method is used in industry because the filter capacitor is able to discharge through the resistor during grid failure [30][31].

$$P_{parallel} = 3\frac{1}{R}\sum_{h}[V_c(h)]^2 \tag{4.12}$$

4.3.2. Active Damping

Active damping techniques inject equal and opposite harmonics onto the power system to cancel those harmonics generated by other equipment. Active damping methods can be classified based on the type of converter, topology, control scheme, and compensation characteristics. The most popular classification is based on the topology, such as virtual resistor, lead-lag compensator and a notch filter. The various active damping techniques that are found in literature are presented in the section. These techniques are vital to decreasing losses when damping is required.

➢ Virtual Resistor

As discussed earlier in section 4.31, resonant oscillations can be damped by connecting a resistance in series or parallel to the filter capacitance or the inductance. In case of a virtual resistance, the control algorithm is developed in such a way to emulate the similar behavior without using a real resistance in the circuit. This method is useful for high power applications where excessive losses can be avoided. According to figure 4.4, the resistance can be connected

at four different positions. However, it is usually preferred to be placed in series or parallel to the filter capacitor. If the virtual resistance is connected in series with the filter capacitance, it requires an extra pair of current sensors to monitor and differentiate the currents. The resulting signals are then again sent to the reference value to compensate the filter resonance. This topology can bring high frequency noise with the amplification of high frequency signals [32][34]. Figure 4.5 shows the implementation of a series virtual resistor.

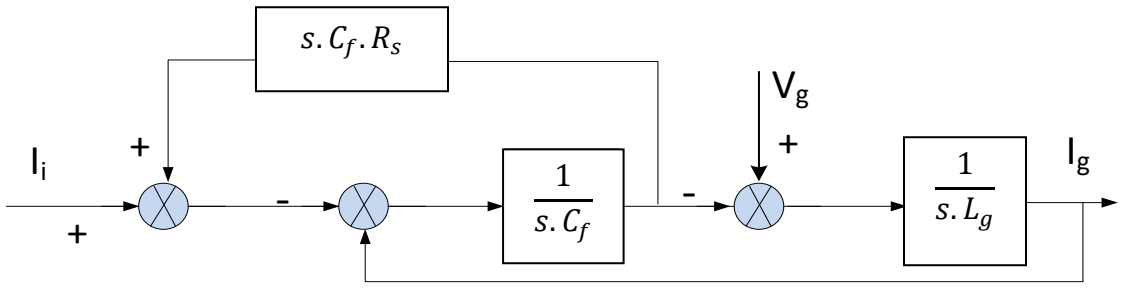


Figure 4.5: Block Diagram of Series Virtual Resistor

Where I_i and I_g are the inverter and grid currents and R_s is the series resistance. In case of a parallel virtual resistor R_p, an amplifier and an extra voltage sensor will be required to monitor the voltages. This technique is more appealing in terms of implementation because it doesn't require a differentiator. Block diagram of the parallel virtual resistor is shown in figure 4.6. Any combination of virtual resistors can be used to achieve required damping.

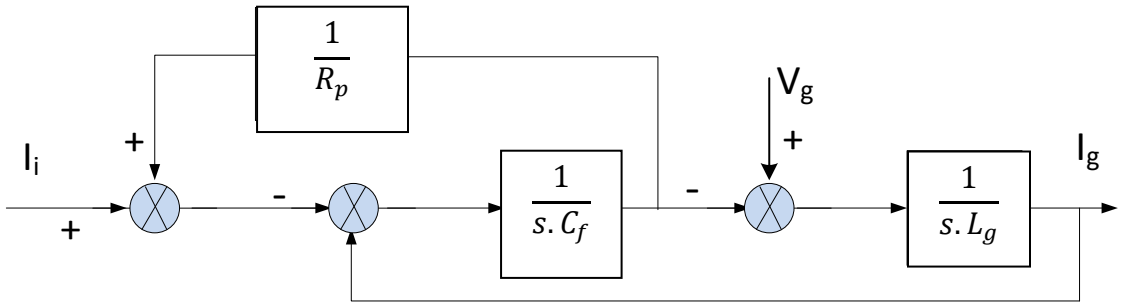


Figure 4.6: Block Diagram of Parallel Virtual Resistor

➢ Lead-Lag Compensator

In order to damp the system a lead-lag compensator normally introduces phase lead into the system. Phase lead can be detected by monitoring capacitor voltages; therefore it requires extra pairs of sensors. These voltages from sensors are then passed through low pass filter and subtracted from the original capacitor voltages, which gives the same high pass filter effect without causing the risk of high harmonic disturbances. The resulting values are subtracted from the input modulated voltage. It brings a small frequency band lead and can be further tuned according to the resonant frequency of the filter. Controlling a lead lag compensator is simple but the overall extra cost of sensors is less influential [31][33]. The transfer function for the lead-lag block is presented in equation 4.13 where the maximum lead angle is given in 4.14 which occurs at frequency mentioned in 4.15. Where k_d and T_d are the gain and time constant of the lead lag transfer function. Figure 4.7 shows the block diagram of the lead lag compensator on load side

$$L(s) = k_d \frac{T_d s+1}{\alpha T_d s+1} \quad , \alpha < 1 \tag{4.13}$$

$$\Phi_{max} = \sin^{-1}\left(\frac{1-\alpha}{1+\alpha}\right) \tag{4.14}$$

$$f_{max} = \frac{1}{T_d\sqrt{\alpha}} \tag{4.15}$$

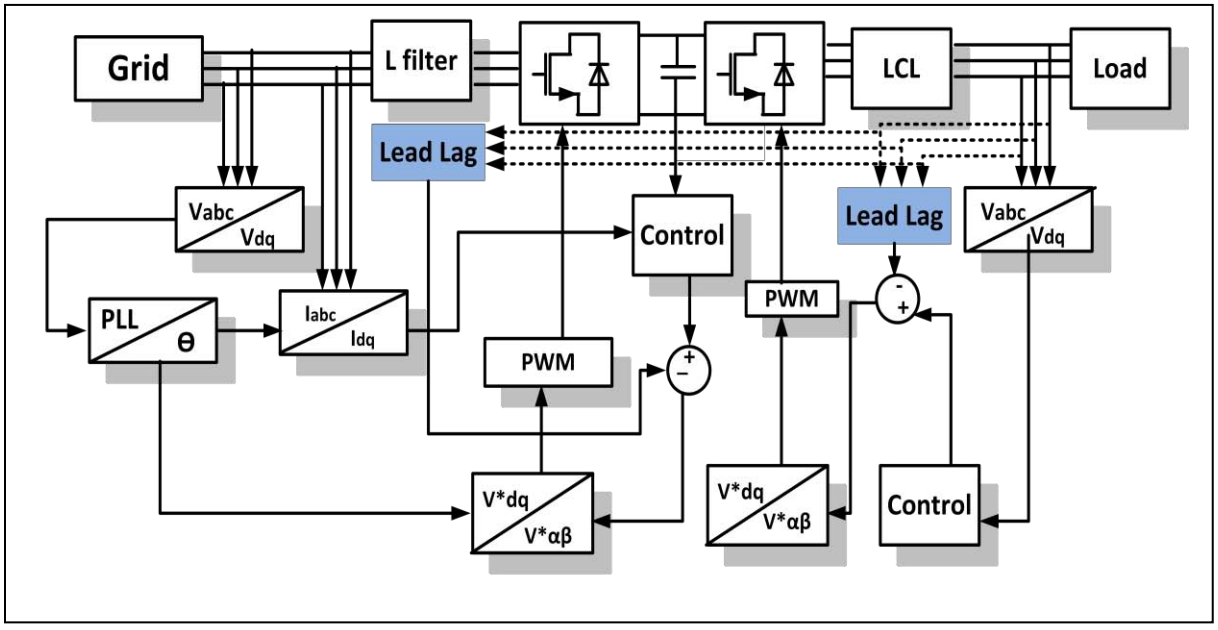


Figure 4.7: Implementation of Lead-Lag Active Damping

➢ Notch and Band stop Filters

A notch filter can be introduced in the current loop to remove the resonant frequency of an LCL filter. Its general transfer function is given below:

$$G = \frac{s^2+2D_z w_z s+w_z^2}{s^2+2D_p w_p s+w_p^2} \tag{4.16}$$

Where D_z and D_p are the zero and pole damping factors respectively and the natural frequencies w_z and w_p are made equal. The pole damping factor should be greater than the zero damping factor to achieve a negative notch. The magnitude and bandwidth of the notch can be determined from the difference between respective damping factors. Figure 4.8 displays the bode plot of a notch filter.

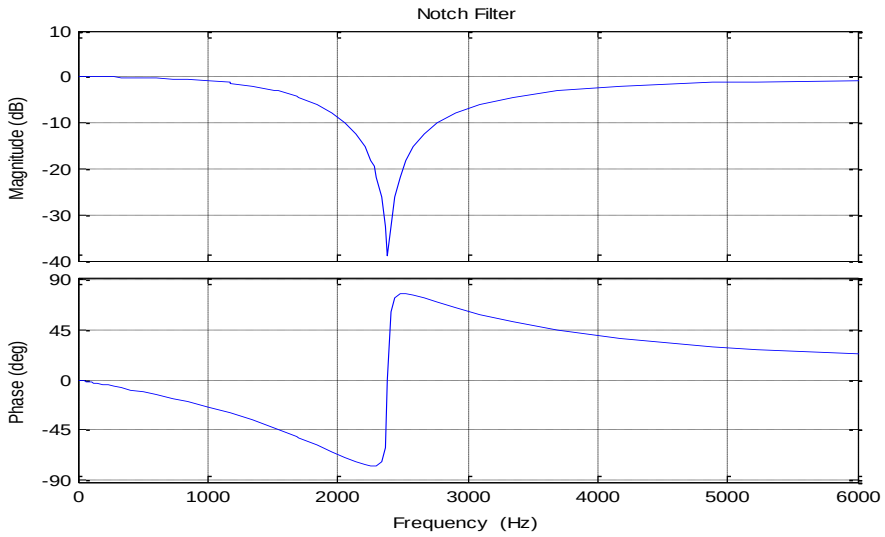


Figure4.8: Notch Filter Bode Plot

The resulted frequency can be tuned to cancel out the resonance introduced by the LCL filter. Band stop filters also have the same effect but can cause high harmonic disturbances. To counteract this, a method is proposed that uses band pass filters and the outputs are subtracted from the inputs. Using either a band stop or notch filter technique does not use extra sensors and can easily be implemented as shown in figure 4.9.

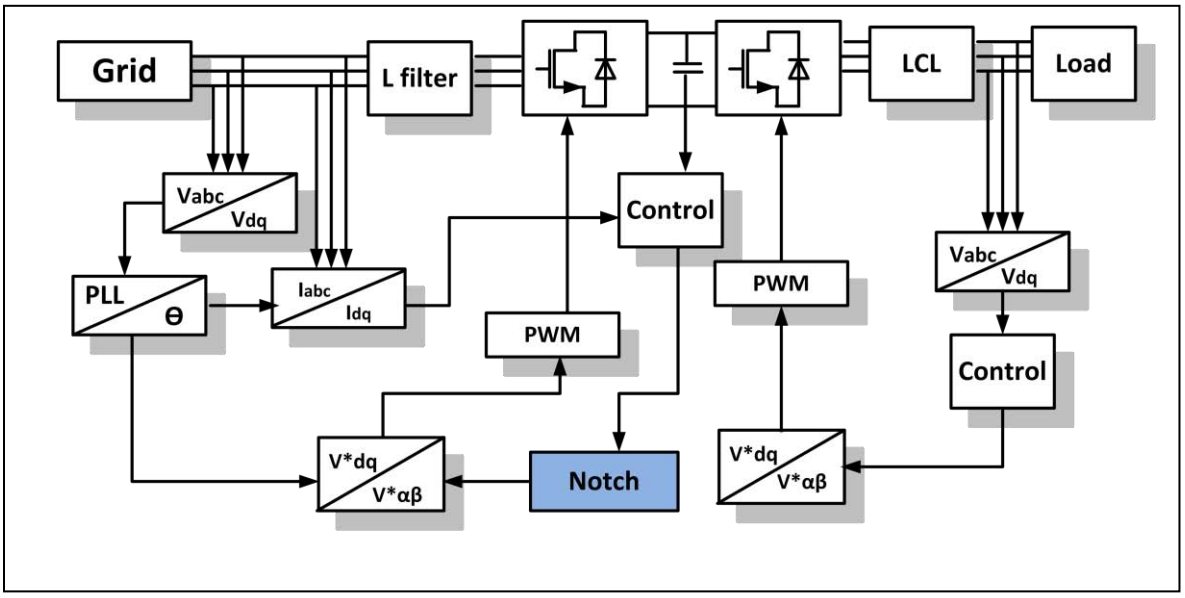


Figure 4.9: Notch Filter Implementation

The resonant frequency of a notch filter changes with variations in grid inductance and filter components, and in that case notch or band stop filter will no longer cancel out the exact resonant frequency. An increase in grid inductance leads to a decrease in resonant frequency and vice versa. Although all the techniques discussed above are attractive options for damping the filter resonance, in this thesis a band pass active damping technique has been applied which can be easily implemented within the control algorithm [34].

4.4. Filtering Method During Unbalance

Voltage Oriented Control (VOC) is dependent on the grid voltages being balanced for optimal control and is based in the synchronous reference frame. If the grid voltages are balanced then the transformation from the stationary *abc* reference frame to the rotating *dq* reference frame results in constant value. If the grid voltage is unbalanced an oscillation is observed, which is due to the presence of a negative sequence component. This negative sequence oscillation rotates at double the fundamental frequency in the positive sequence reference frame. In figure 4.10 a per unit direct axis voltage waveform is shown for both balanced and unbalanced (type-B dip) situations.

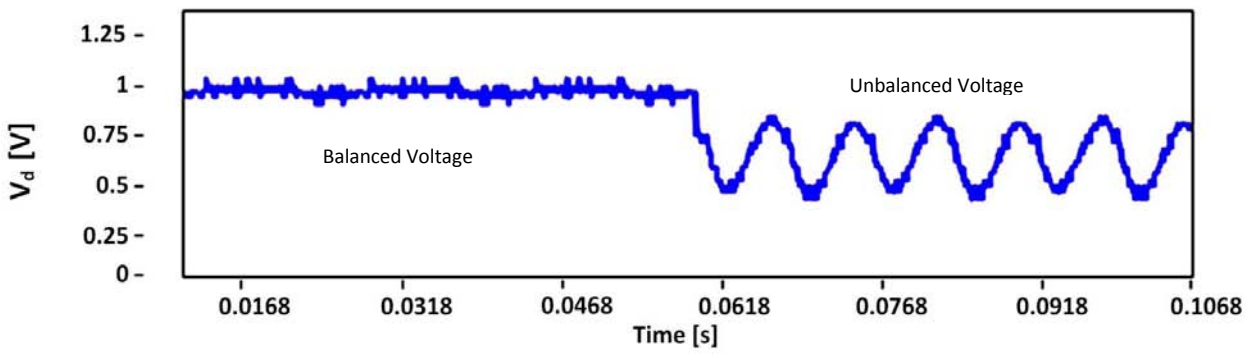


Figure4.10: Comparison for Balanced and Unbalanced Voltages

Figure 4.11 is the zoomed-in screen shot of the type-B dip area and can be used to determine the frequency of oscillation i.e 100Hz which is twice the fundamental frequency.

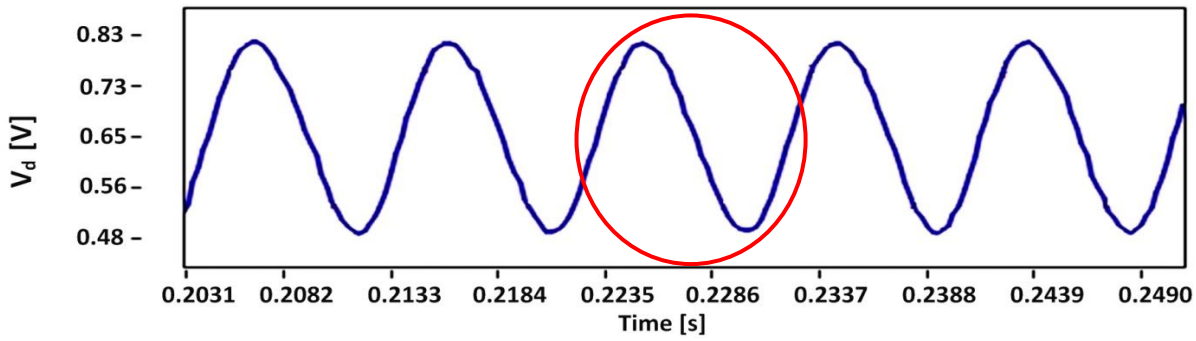


Figure 4.11: Unbalance in Case Type-B Dip Implementation

Figure 4.12 is the space vector diagram for unbalanced voltages where the resultant voltage vector is composed of positive and negative sequence components. The positive and negative vectors rotate in opposite directions. The resulting effect is an oscillation at twice the rotating frequency when observing from either the positive or negative reference frame.

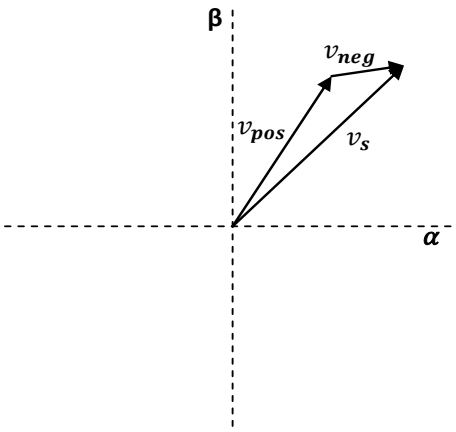


Figure 4.12: Positive and Negative Components in Rotating Reference Frame

In figure 4.13 the outer circle shows a perfectly balanced voltage whereas the oval depicts an unbalanced voltage when a type-B dip is implemented on the system. The shape of the oval is dependent on the severity of the dip.

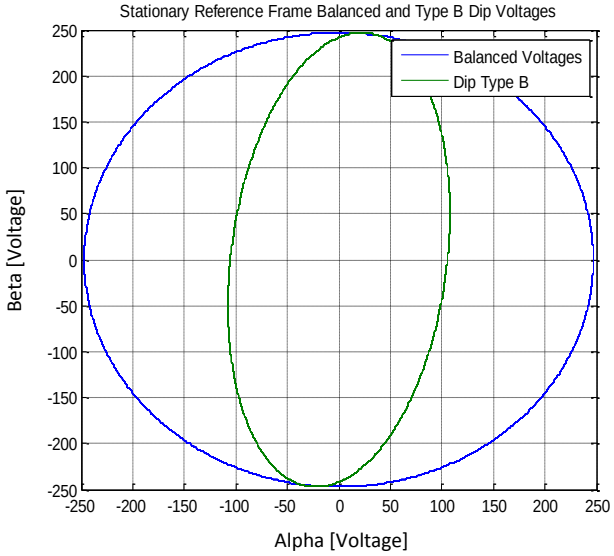


Figure 4.13: Effect of Voltage Unbalance in the Stationary Reference Frame

4.4.1. Filtering with Sequence Separation Method

In the case of unbalance a negative sequence appears in the rotating reference frame as previously discussed. In order to extract this sequence the following procedure is used. The three phase voltage *abc* is transformed into the αβ reference frame. The transformations into the positive and negative *dq* reference frames are then made with the help of equations 4.17 and 4.18. In the positive reference frame the positive sequence component is a DC value and the negative sequence component can be filtered out by using a simple low pass filter.

Figure 4.14 illustrates the sequence extraction method. The transient response of this method is comparatively slower than signal cancellation method because of the low pass filter cut-off frequency [35][36]. Due to its simple implementation this technique has been applied in this thesis and detailed control is discussed in the next chapter.

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} \quad (4.17)$$

$$\begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} \quad (4.18)$$

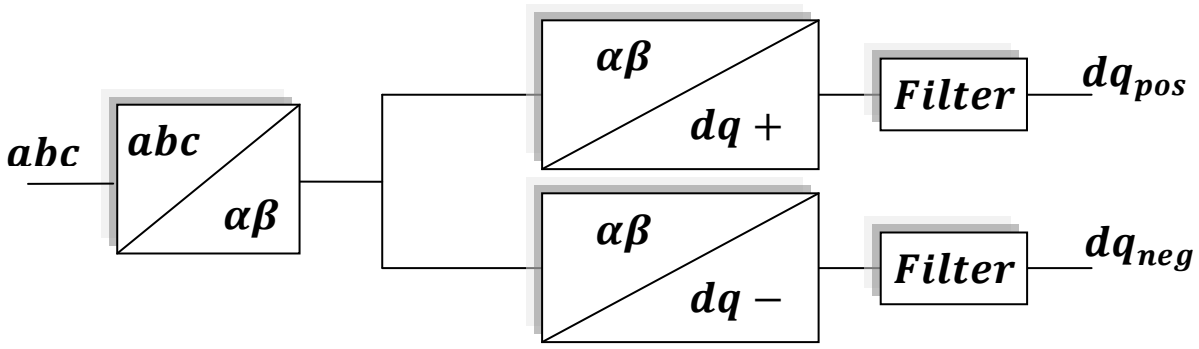


Figure 4.14 : Filter Sequence Separation Method

4.5. Filter Design

The main purpose of this filter is to reduce the current ripples produced by harmonics at the switching frequency. To simplify the control of this project, the following limitations have been taken into account.

- Decrease in power factor restricts the capacitance value, which has to be less than 5% at the rated power.
- The total value of the inductance should be less than 0.1 per unit to limit the voltage drop across the filter. If the voltage drop is too large, a higher DC bus voltage would be required, resulting in increased switching losses. The voltage drop across the inductor can be given as 4.19.

$$V = L\frac{di}{dt} \tag{4.19}$$

- The resonant frequency of the filter should be higher than ten times the fundamental frequency and half of the switching frequency.

Base values which are the percentage of actual filter values, are calculated from equations 4.20, 4.21 and 4.22 below.

$$Z_b = \frac{(E_n)^2}{P_n} \tag{4.20}$$

$$L_b = \frac{Z_b}{\omega_n} \tag{4.21}$$

$$C_b = \frac{1}{\omega_n Z_b} \tag{4.22}$$

Where E_n is the line-to-line voltage, P_n – rated power and ω_n – fundamental frequency

Limitation 1 sets the maximum capacitor value to:

$$C_f = xC_b \tag{4.23}$$

Where x is the percentage of reactive power absorbed under rated conditions

In accordance with limitation 2, the maximum total inductance value is determined by

$$L_{max} = L_b(0.1) \tag{4.24}$$

The converter and grid inductors can be related by r

$$L_g = rL_I \tag{4.25}$$

The ripple current should be attenuated to a maximum value of 0.2 times converter side ripple current. Converter side inductance can be calculated as

$$L_I = \frac{V_{DC}}{8\Delta i \omega_{sw}} \tag{4.26}$$

Where V_{DC} is DC-Link voltage, Δi is ripple current attenuation i.e 20% of I_n and ω_{sw} is the switching frequency.

The attenuation is set by choosing a suitable value of "r" between the inverter and grid currents at switching frequency harmonic h_{sw} in equation 4.27.

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{1}{|1+r(1-a.x)|} \tag{4.27}$$

Where $a = L_I C_b {\omega_{sw}}^2$

Once all of the component values have been chosen, the resonant frequency of the filter can be calculated with equation 4.28.

$$F_{res} = \frac{1}{2\pi}\sqrt{\frac{L_t}{L_I.L_g C_f}} \tag{4.28}$$

Where $L_t = L_I + L_g$ and is the total inductance of the LCL filter.

After calculating all the components values. R, which is the passive resistance is determined and will only be applied if passive damping is needed. It is equal to $\frac{1}{3}$ of the capacitor impedance at the resonant frequency and can be applied in parallel to the capacitor.

$$R = \frac{1}{3\omega_{res} C_f} \tag{4.29}$$

4.5.1 Calculated Filter Values

The filter component values are determined using the steps and calculations presented above and are presented in table 4.1 below.

Table 4.1: System Rated Parameters

Parameter	Value
V_{LL}	$380V$
P_{rated}	$30kW$
$F_{switching}$	$10kHz$

Table 4.2 shows the calculated component values for the LCL filter:

Table 4.2: Calculated Filter Components

Parameter	Value
Z_b	4.81Ω
L_b	$15.3\mu H$
C_b	$662\mu F$
C_f (x = 5%)	$33.1\mu F$
L_I	$12.5mH$
r	0.3
L_g	$3.75mH$
f_{res}	$515.6Hz$
R	3.1Ω

The magnitude of "r" is obtained by selecting an attenuation value from figure 4.15 which is a graphical representation of equation 4.27. It shows the attenuation value as "r" is increased.

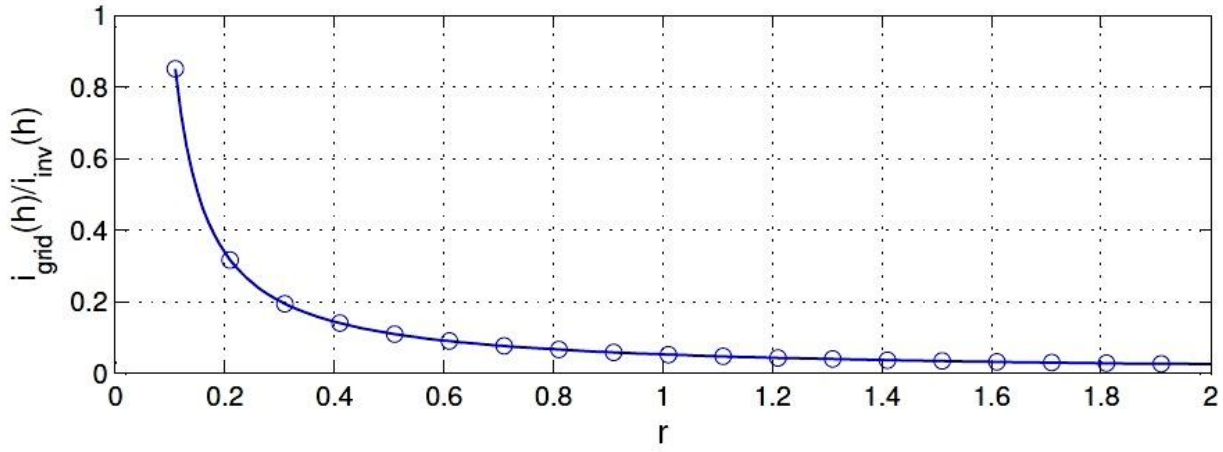


Figure4.15: Relationship Between Attenuation and "r"

A value of 0.3 was selected to obtain an attenuation magnitude of less than 20%.

A bode plot of the designed filter is presented in figure 4.16.

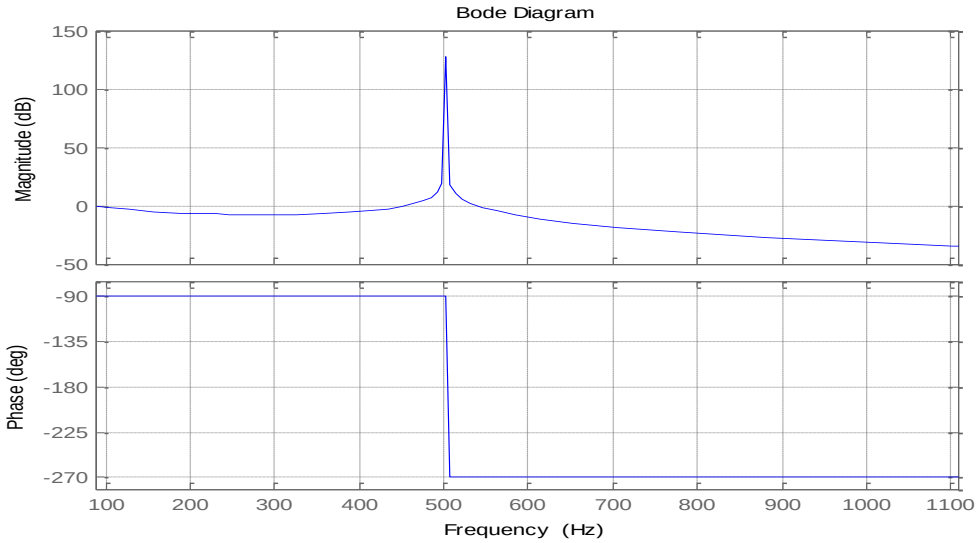


Figure 4.16: Bode Plot of LCL Filter

Figure 4.16 indicates that the resonant frequency is located near 510 Hz which is within the design limits. Furthermore, the attenuation at the switching frequency is greater than 50 dB,

which shows the resonant frequency will have a higher gain and needs to be damped using passive or active technique described in section 4.3.

4.6. DC – Link Design

The first step in sizing the DC-link is to understand how much capacitance is required for the application. Design criteria generally depend on the maximum DC-link voltage required for given inverter design and on the short time peak power generation. For three-level converter as an active rectifier the sizing of the capacitors should be done with respect to the mid-point voltage variation. The DC-link design using electrolytic capacitors is always limited by the maximum ripple current. It depends on how much current ripple a capacitor can sustain and how many individual capacitors are required to meet the design criteria. Maximum ripple current only occurs at 50% of the duty cycle. Moreover, the design also depends on the amount of ripple voltage and ESR values of the capacitor. Although this thesis does not attempt every consideration for designing the DC-link, It has discussed how the load power and maximum ripple voltage affect the sizing of the capacitors for the DC-link [37][38].

If the energy reserve in the DC-link is E_{DC} and an overload condition is assumed for double the nominal load i.e $P_{\max} = 2P_n$ given $t = 0.5\text{s}$, then the energy reserve can be $E_{DC} = 15kWs$.

$$E_{DC} = (P_{\max} - P_n).t \tag{4.30}$$

Where P_n was considered 30kW. The filter capacitor was selected based on the following equation and on the availability of nominal and maximum DC-link voltages. The final value was chosen as 39.2mF which was closest to the estimated value. Where C_{DC} is the DC-link capacitance, $V_{DC,n} = 800$ and $V_{DC,\max} = 1.5xV_{DC,n}$.

$$C_{DC} = \frac{2xE_{DC}}{V^2_{DC,\max} - V^2_{DC,n}} \tag{4.31}$$

4.7. Conclusion

This chapter described a gradual scheme of the LCL filter design. The transfer function was derived with the help of equivalent circuit diagram. Passive and active damping techniques were discussed in detail. This thesis will employ a band pass active damping technique due its simplicity and lack of extra components. For an unbalanced voltage condition a sequence separation method was used to investigate both positive and negative sequences. Filter components were then precisely determined. The DC-link capacitor value was estimated on the basis of maximum voltage requirements.

CHAPTER 5

CONTROL DESIGN

This chapter introduces the control system design. Two tuning techniques are discussed for the PI controllers tuning. Transfer functions are then developed for both grid and load side of the emulator including the DC link. Stability of the controller is shown with the help of root locus plots done in MATLAB Sisotool.

5.1. Control Techniques

Among grid connected systems, the controlled power flow plays an important role in the system's performance and it largely depends on the applied control technique. In the last two decades many researchers have been encouraged to propose a method that assures less harmonic distortion, high dynamic response and better DC voltage regulation. Different current control techniques have been described for different applications. As this thesis deals with controlling the unbalanced voltages and the current is oriented along the active voltage component (i.e V_d) voltage oriented control is therefore implemented. A comparison on different control techniques is shown in the table 5.1.

Table 5.1: Comparison of the Control Techniques

Control Technique	Stability	Harmonic Content	Dynamic Response	Simplicity
Ramp-Comparison	Dependant on load parameters	Well defined harmonic spectrum	Slow	Relatively simple
Hysteresis	Robust	Spread harmonic spectrum	Extremely fast	Complex
Voltage Oriented	Dependant on load parameters	Well defined harmonic spectrum	Fast	Relatively simple
Direct Power	Robust	Spread harmonic spectrum	Extremely fast	Simple
Predictive Current	Dependent on load parameters	Well defined harmonic spectrum	Fast	Complex Analytical Approach

From the table it can be seen that the voltage oriented control has a well defined harmonic spectrum and is relatively simple to implement. Moreover, with the help of voltage oriented control independent control on active and reactive current components can be achieved which corresponds to a direct control on the power flow and is beneficial for the grid connected applications.

5.1.1. Voltage Oriented Control

VOC uses rotating *dq* reference frame theory to ensure zero steady state error. By transforming AC values to DC equivalent values, the infinite gain of the PI controllers drives the *dq* values to the desired references without errors.

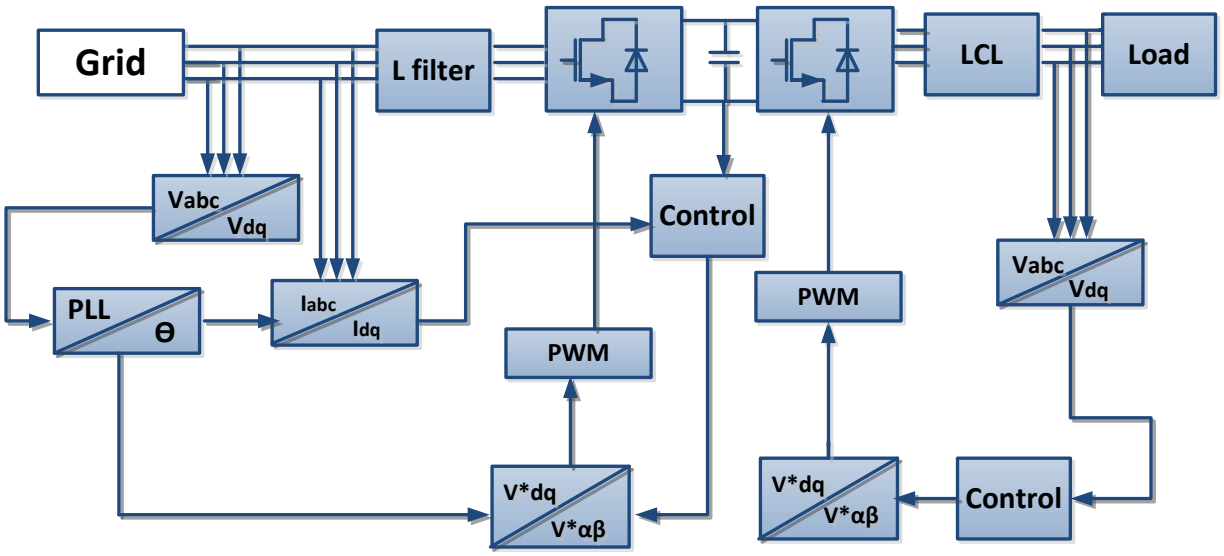


Figure 5.1: Control Scheme of the Grid Emulator

Figure 5.1 illustrates the VOC principle involving the rotating reference frame components. The three phase grid voltage is converted to *dq* components using synchronous reference frame transformations. Two sets of PI controllers are located inside the control blocks which regulate any existing errors by generating appropriate V^*_{dq} controlled values. These values are further used to generate PWM signals for the power devices.

Although VOC allows control on the active and reactive power by using two distinct inner and outer loops, the control of the variables is not defined independently. For this, a dual vector control is employed to gain control on each component properly and is discussed in section 5.5.

5.2. Control Tuning Techniques

Different tuning techniques are implied for calculating the controller gain values. In literature the most common methods implemented for similar systems are the modulus optimum and the symmetrical optimum.

5.2.1. Modulus Optimum

This technique is used for conventional analog controller tuning. If a system has one major time constant and one minor time constant then the standard form of the transfer function for the modulus optimum can be achieved by cancelling the dominant time constant. In the system of figure 5.2, the modulus optimum attempts to comply with the following set of rules by tuning the controller parameters [39]:

$$G_{ry}(0) = 1 \tag{5.1}$$

Where G_{ry} is the closed loop transfer function

$$\frac{d^m|G_{ry}(j\omega)|}{d\omega^m} = 0 \text{ , at } \omega = 0 \tag{5.2}$$

and ω is the frequency of natural oscillation

In other words, the closed loop transfer function gain should be larger than unity for as high frequency as possible. From the equations 5.1 and 5.2 the first step is to find out the order of the transfer function and then compare to the equations given below. The second and third order modulus optimum transfer functions are:

$$G_{MO}(s) = \frac{1}{1+\sqrt{2}T_{MO}s+T_{MO}^2s^2} \tag{5.3}$$

$$G_{MO}(s) = \frac{1}{(1+T_{MO}s)(1+T_{MO}s+T_{MO}^2s^2)} \tag{5.4}$$

Where T_{MO} is the time constant of the feedback control system designed by this control method. However, the system can be further tuned to the desired value of the cross-over frequency by selecting the constant gain term. [39].

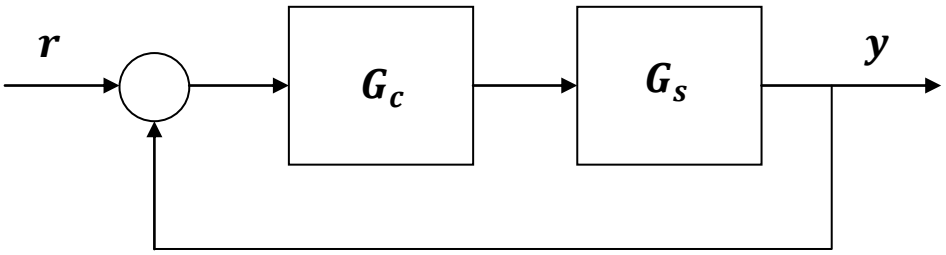


Figure 5.2: General Control Loop

5.2.2. Symmetrical Optimum

As the previous technique was based on a pole cancellation method, therefore in this case when one of the poles is already near to the origin, the pole replacement doesn't change the situation. In symmetrical optimum design procedure the controller pushes the frequency response of the system as low as possible. It is standard for the controllers open loop transfer functions with a double integration term, and is based on the general equation below [40]:

$$A_i = a_i^2 + 2\sum_{j=1}^{i}(-1)^j a_{i-j} a_{i+j} \tag{5.5}$$

The calculation of the control parameters is based on the set of equations:

$$A_i = 0 \tag{5.6}$$

$$i = 1,2,\ldots,m \tag{5.7}$$

Where i is the number of adjustable controller parameters.

A PI controller has two adjustable parameters which give the following two equations

$$A_1 = a_1^2 - 2a_0a_2 = 0$$

(5.8)

$$A_2 = a_2^2 - 2a_1a_3 = 0$$

(5.9)

In [40] the equation is modified in order to ensure the maximum phase margin

$$a_1^2 = \beta^{\frac{1}{2}}a_0a_2$$

(5.10)

$$a_2^2 = \beta^{\frac{1}{2}}a_1a_3$$

(5.11)

Value of β can be chosen in such a way that if it is less than 4, the phase margin it generates is less than 40° which is less practical. Whereas, for a higher value of β the phase margin increases beyond 60° which is not always preferable. As phase margin increases for the given frequency, the system can compensate more delays. In [42] a fact is used that a value of $\beta < 9$ results in one real and two imaginary poles which form a conjugate pair. The equation 5.12 shows the relationship between the damping factor and the variables that set the pole positions.

$$s^3 + (\alpha + 2)\sigma s^2 + \left(2\alpha + 1 + \frac{1-\zeta^2}{\zeta^2}\right)\sigma^2 s + \left(1 + \frac{1-\zeta^2}{\zeta^2}\right)\sigma^3$$

(5.12)

Where $\alpha > 1$ and ζ is the damping factor. Equation 5.12 is then compared to the third degree characteristic equation presented in equation 5.13 which can then be used to determine the controller parameter values.

$$a_3 s^3 + a_2 s^2 + a_1 s + a_0 \quad (5.13)$$

5.3. PI Controllers

The control algorithms for both the grid and load sides of the back-to-back converters are discussed in this section. Two control loops are studied in detail and gain values are calculated. This section also illustrates how the PI controllers for the respective loops are tuned. Two tuning techniques, modulus optimum and symmetrical optimum are implemented for both the inner and the outer loops.

5.3.1. Grid Side Control

Figure 5.3 illustrates the grid side control for the grid emulator system. Three PI controllers are used consisting two inner current loops and an outer voltage loop for DC bus voltage regulation.

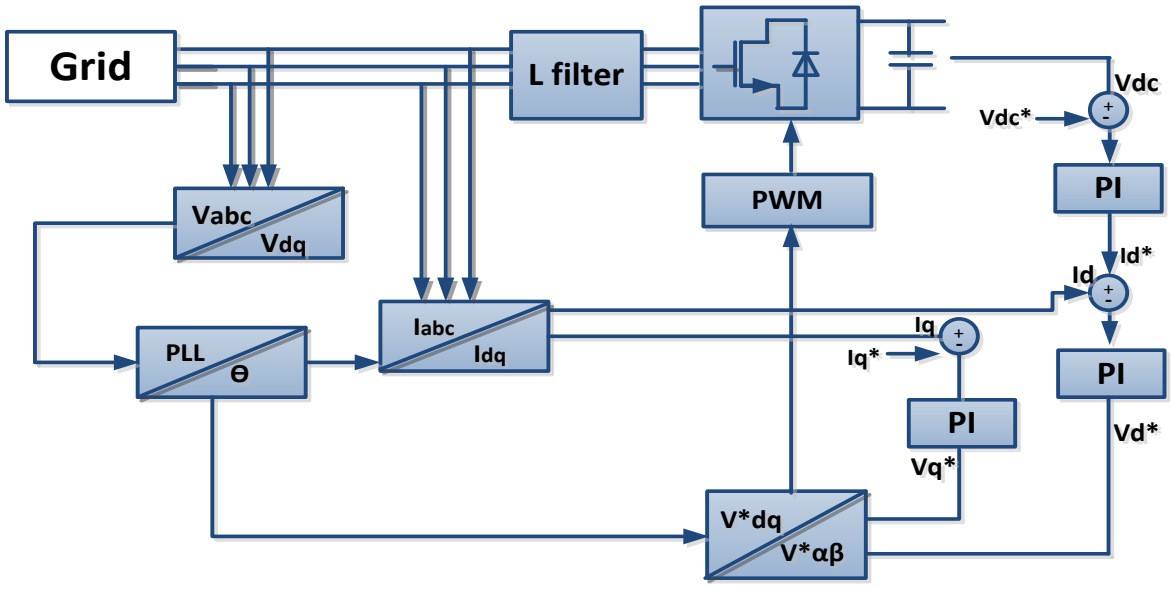


Figure 5.3: Grid Side Control Scheme of the Emulator

Only a single current loop is needed to be tuned because they have the same responses. The UPF control technique uses the d-axis current and sets the q-axis current to zero assuring zero reactive power, therefore the d-axis current is used to tune the controller. The block diagram for the current loop is shown in figure 5.4.

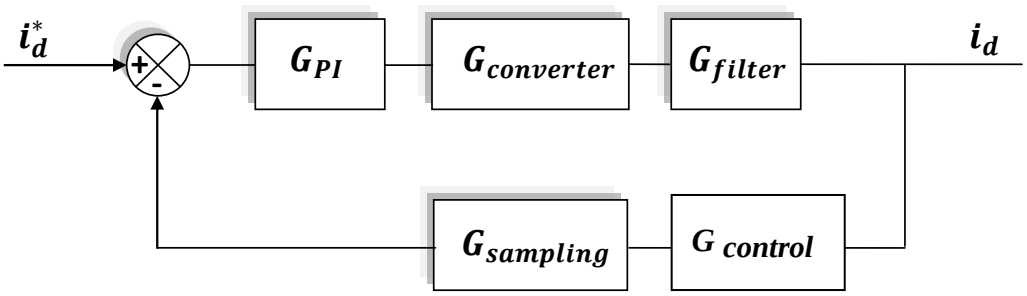


Figure 5.4: Grid Current Loop Block Diagram

Transfer functions of the system components are listed below:

- Transfer function for the PI controller

$$G_{PI} = K_p + \frac{K_i}{s} \tag{5.14}$$

- Transfer function for the control algorithm

$$G_{control} = \frac{1}{1 + sT_s} \tag{5.15}$$

Where $T_s = {}^{1}/_{f_s}$ and $f_s = 10kHz$ is the sampling frequency

- Transfer function for the converter block

$$G_{converter} = \frac{1}{1 + s0.5T_{sw}} \tag{5.16}$$

Where $T_{sw} = {}^{1}/_{f_{sw}}$ and $f_{sw} = 10kHz$ is the switching frequency.

- The transfer function of the filter can be approximated by ignoring the filter capacitance and its transfer function is as follows:

$$G_{Filter} = \frac{1}{Ls + R} \tag{5.17}$$

Where $L = L_i + L_g$ and $R = Ri + Rg$, R is the sum of the parasitic resistances.

- Transfer function for the sampling block

$$G_{sampling} = \frac{1}{1 + s0.5T_s} \tag{5.18}$$

To simplify the transfer function of the loop, the small time constants $T_{sampling}$ and $T_{switching}$ can be combined into a single delay, T_c. The closed loop characteristic function of the system is

$$G_{current} = G_{PI}.G_{control}.G_{converter}.G_{filter}.G_{sampling} \tag{5.19}$$

After solving it gives,

$$G_{current} = \frac{1}{2sT_c(1 + sT_c)} \tag{5.20}$$

Using the modulus optimum method to tune the PI controller the gains are determined by equations 5.21 and 5.22 below.

$$K_p = \frac{T_E}{2K_E T_c} \tag{5.21}$$

$$K_i = \frac{K_p}{T_E} \tag{5.22}$$

Where $K_E = \frac{1}{R}$ and $T_E = \frac{L}{R}$

The gain values that are obtained by these equations are indicated below and the pole placement method is used to start the discrete analysis in sisotool.

$$K_p = 20\,, \quad K_i = 769.2$$

Two requirements are imposed on the current controller: the phase margin should be larger than 40° and gain margin larger than 6 *dB*. The proportional gain K_p is moved until damping of 0.707 is achieved, which is shown in figure 5.5 with resulting gains of:

$$K_p = 1.5, \quad K_i = 576$$

The current controller gains are reduced because the output from the *dq* transformation block produces an oscillation at twice the grid fundamental frequency. Damping of the resonant poles and the zero pole map is also shown in the figure 5.5. It shows that the systems has poles at the damping factor of 0.70 and are within the unit circle.

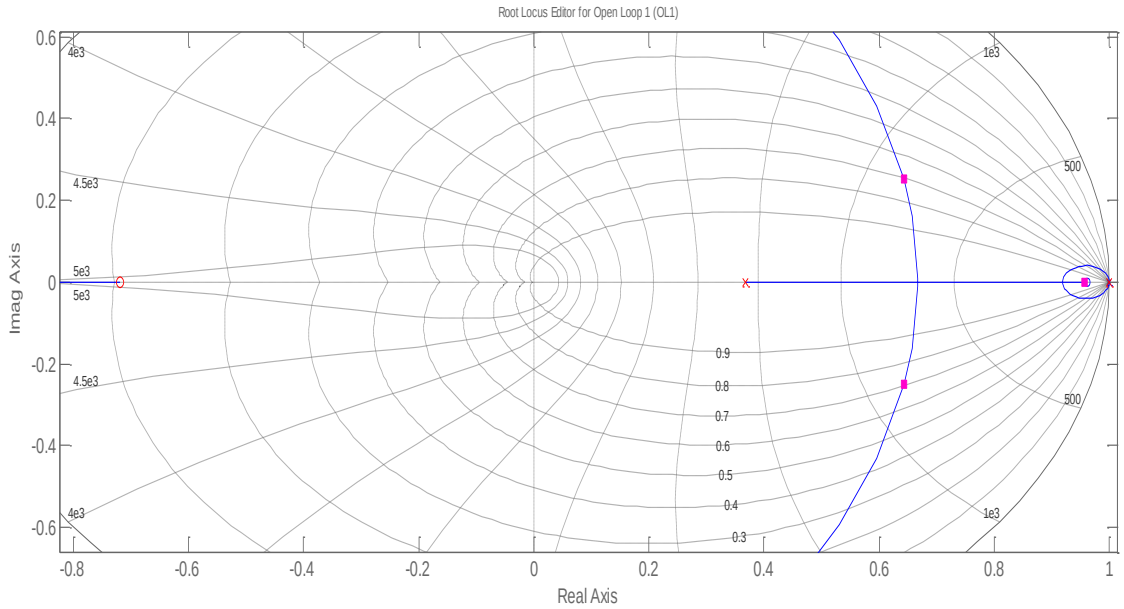


Figure 5.5: Grid Current Loop Root Locus

More information of the system stability can be extracted from figure 5.6, which shows a bode plot of the open-loop current control and its step response.

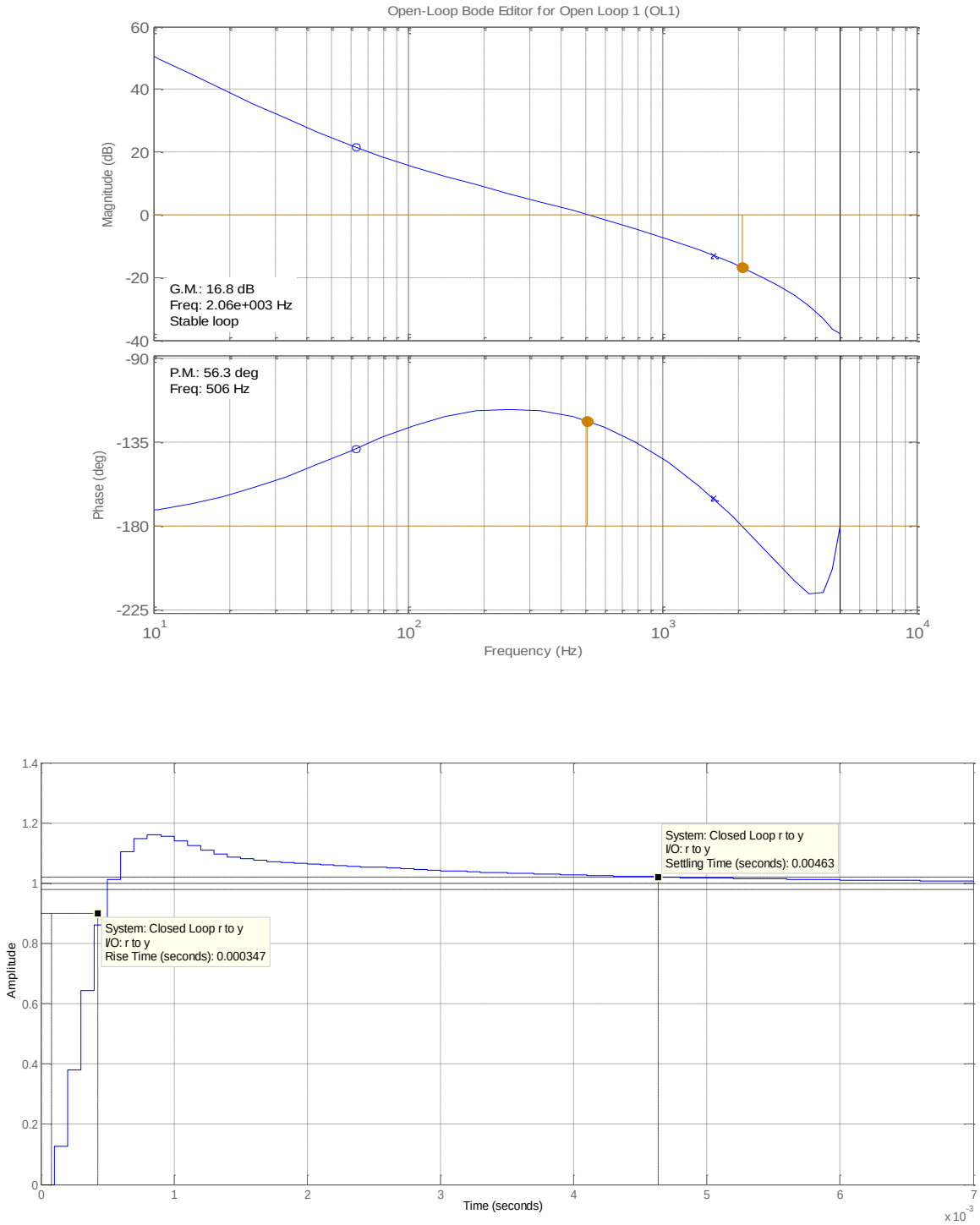


Figure 5.6: Grid Current Loop Bode Plot and its Step Response

Bode plot shows the gain margin of 16.8 *dB* and phase margin of 56.3°. Rise time of 0.347ms and settling time of 4.6ms can also be observed in the above figure, indicating that the loop is stable.

5.3.2 DC Link Voltage Control

The DC voltage is controlled by the exchange of power in the converter. The change in DC voltage depends on the power drawn from or into the grid by changing the reference of the inner current control loop. The internal and external loops are considered decoupled, therefore the actual grid currents are considered to be equal to their references. The DC voltage controller is tuned by using symmetrical optimum technique before a discrete analysis is carried out using Sisotool.

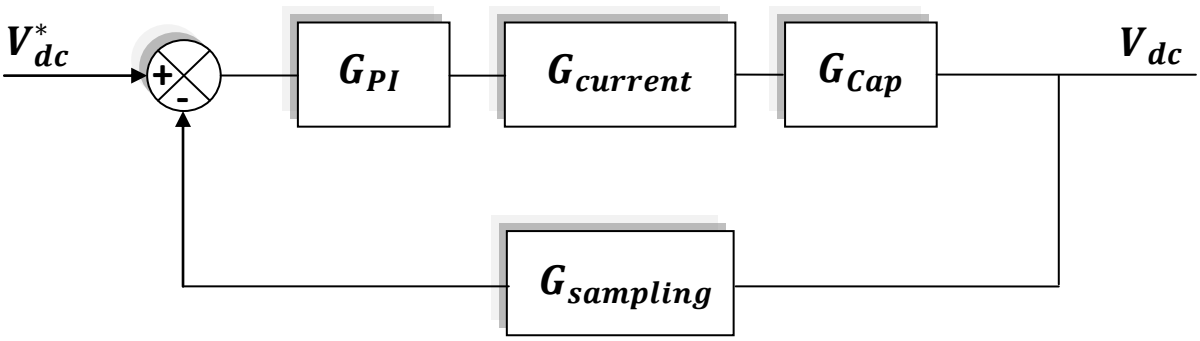


Figure 5.7: DC Link Voltage Loop Block Diagram

The outer DC Link Voltage control loop block diagram is illustrated in figure 5.7. The values of the PI controller are calculated below:

$$G_{cap} = \frac{1}{Cs} \tag{5.23}$$

$$G_{current} = \frac{1}{3sT_s+1} \tag{5.24}$$

A phase margin ϕ of 45^0 Is imposed for the voltage loop at the crossover frequency (ω_{cr}).

$$a = \frac{1+cos\phi}{sin\phi} \tag{5.25}$$

Where 'a' is the symmetrical distance between T_s and ω_{cr},

The PI gains can be calculated as,

$$K_p = \frac{4C_{dc}}{2T_c{}^2 9aT_s} \tag{5.26}$$

$$K_i = \frac{K_p}{3a^2T_s} \tag{5.27}$$

The gain values that are determined by these equations are:

$$K_p = 5.8, \quad K_i = 341.2$$

These values are again used as a starting point for the discrete analysis in the Sisotool toolbox and the gain values are changed by the damping factor of 0.707 to:

$$K_p = 0.5, \quad K_i = 294$$

Figure 5.8 is the open loop root locus diagram of the DC link voltage loop and shows the poles at a damping factor of 0.707 within the unit circle suggesting system stability.

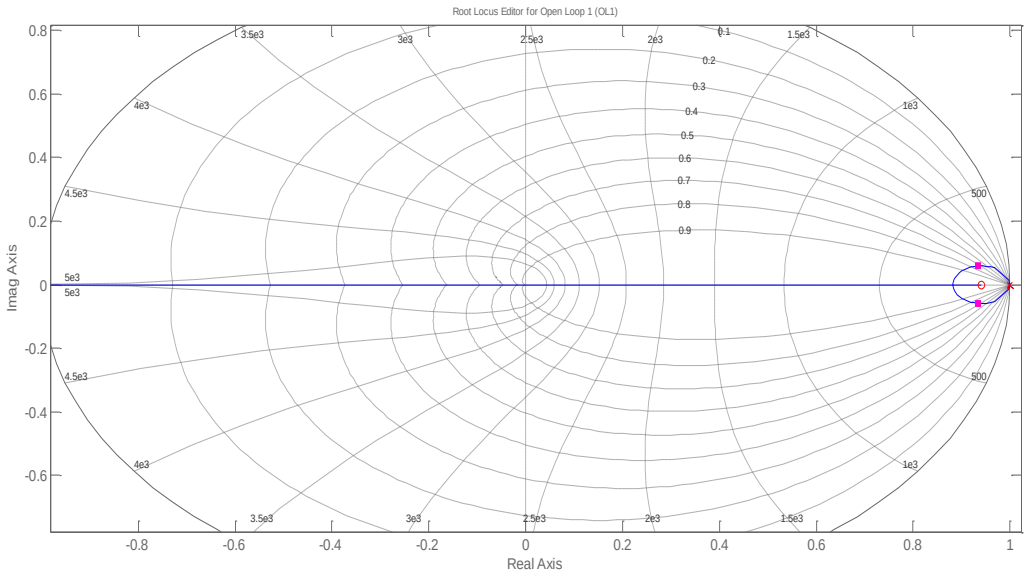


Figure 5.8: DC link Voltage Loop Root Locus

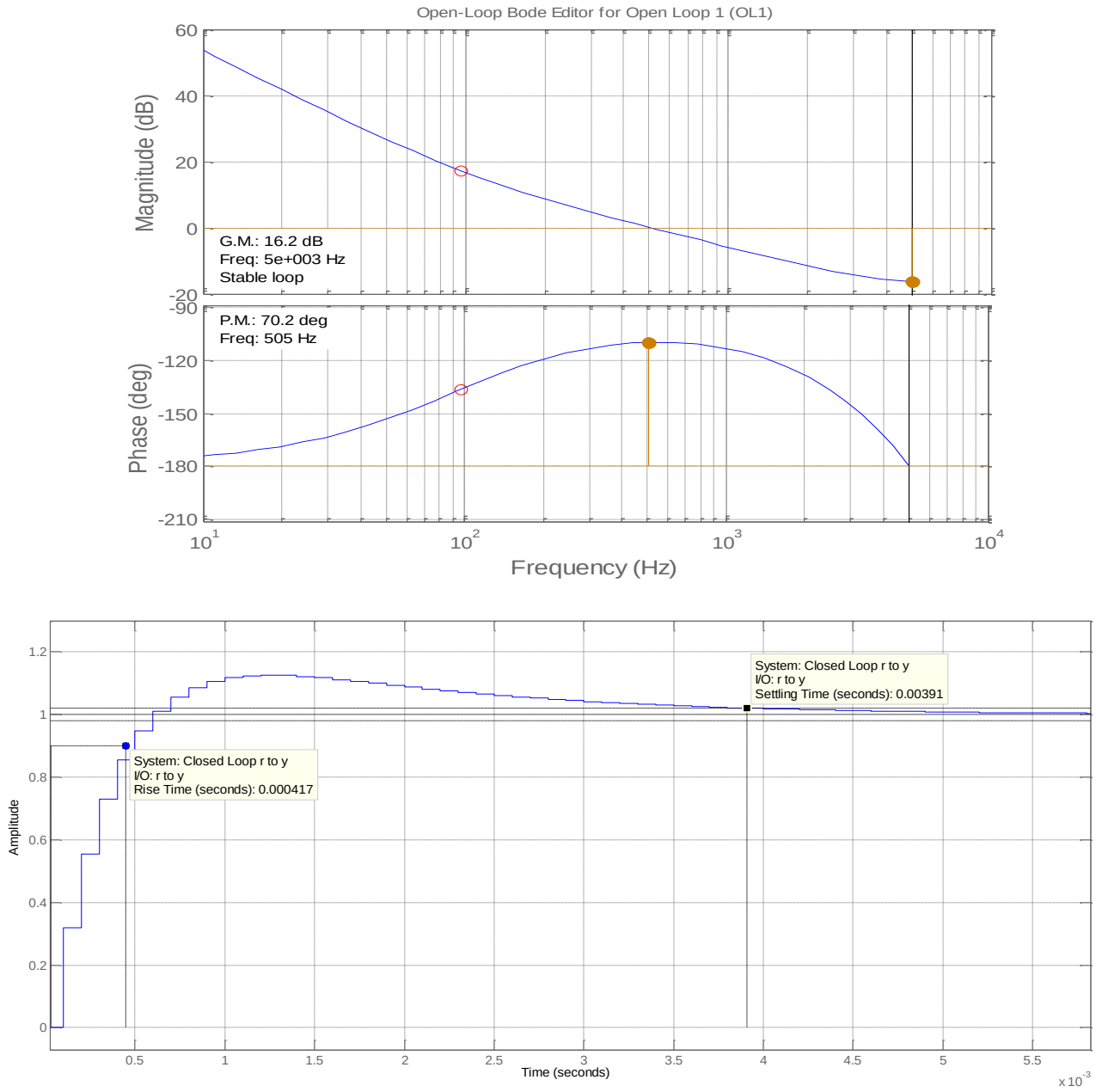


Figure 5.9: DC Link Voltage Loop Bode Plot and Step Response

A gain margin of 16.2 *dB* is achieved with phase margin of 70.2°. A quick step response is observed with a rise time of 0.41ms and settling time of 3.9ms.

5.3.3. Load Side Control

The load side control for the grid emulator is shown in figure 5.10. Two PI controllers are used for independent load voltage regulation.

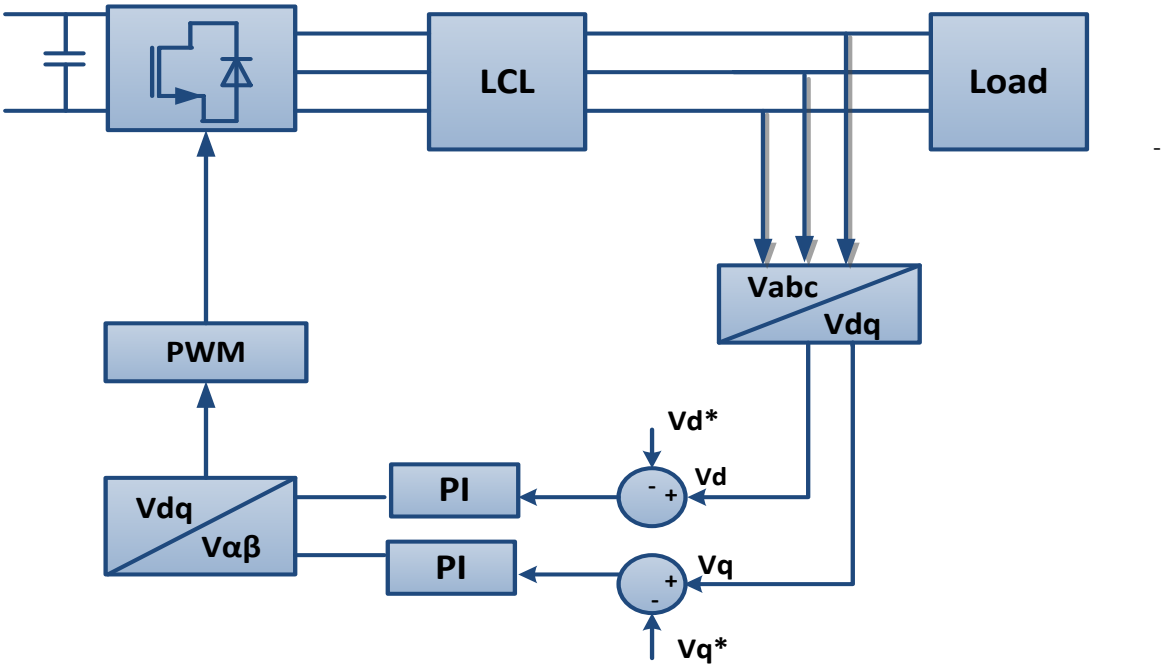


Figure 5.10: Load Side Control Scheme of the Emulator

Again a single control loop is tuned because the other has the same response and same gain values are used for desired voltage regulation. Block diagram for the voltage loop is shown in figure 5.11.

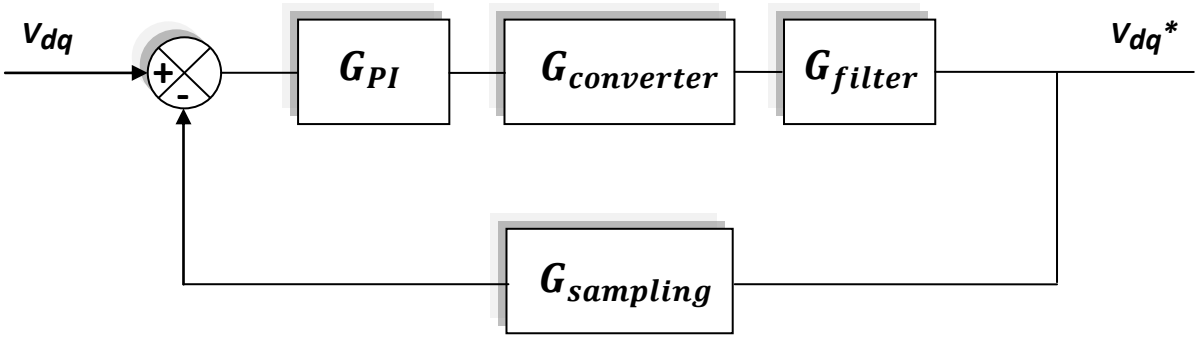


Figure 5.11: Load Side Voltage Loop Block Diagram

Transfer functions for the PI controller, control algorithm, converter block, filter and sampling block are given in equations 5.14, 5.15, 5.16, 5.17 and 5.18.

The closed loop characteristic equation is:

$$G_{voltage} = \frac{1}{2sT_c(1 + sT_c)}$$

(5.28)

Using the modulus optimum method to tune the PI controller the gains are determined by equations 5.29 and 5.30.

$$K_p = \frac{T_E}{2K_E T_c}$$

(5.29)

$$K_i = \frac{K_p}{T_E}$$

(5.30)

The gain values that are obtained by these equations are indicated below and the pole placement method is used to start the discrete analysis in Sisotool.

$$K_p = 38.2, \;\; K_i = 757.5$$

The poles are moved until damping of 7.07 is achieved and the resulting gains are:

$$K_p = 1.5, \;\; K_i = 293$$

Figure 5.12 is the open loop root locus diagram of the load voltage control loop and shows the poles located at a damping factor of 0.707 within the unit circle confirming system stability.

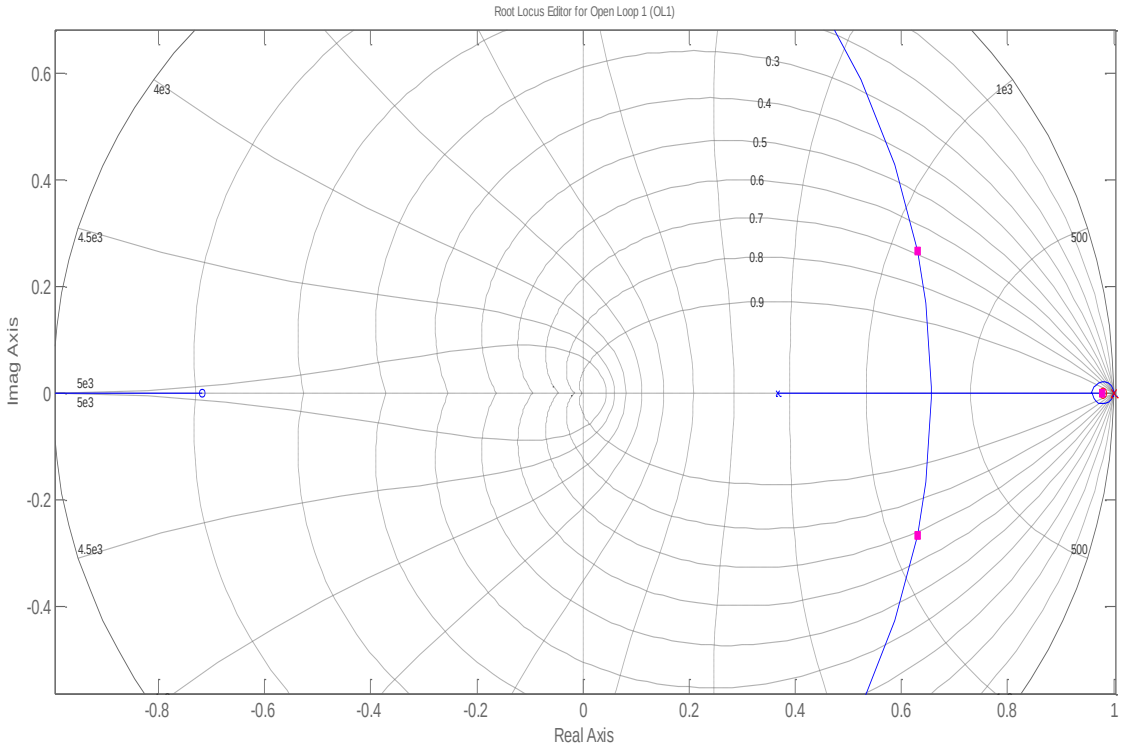
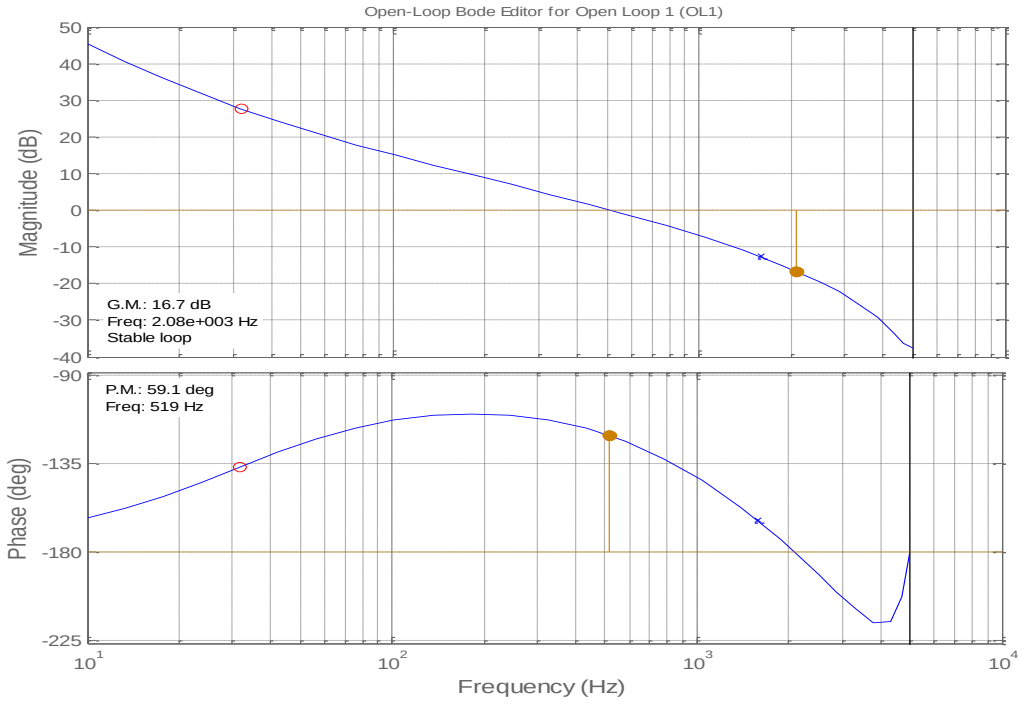


Figure 5.12: Load Side Voltage Loop Root Locus



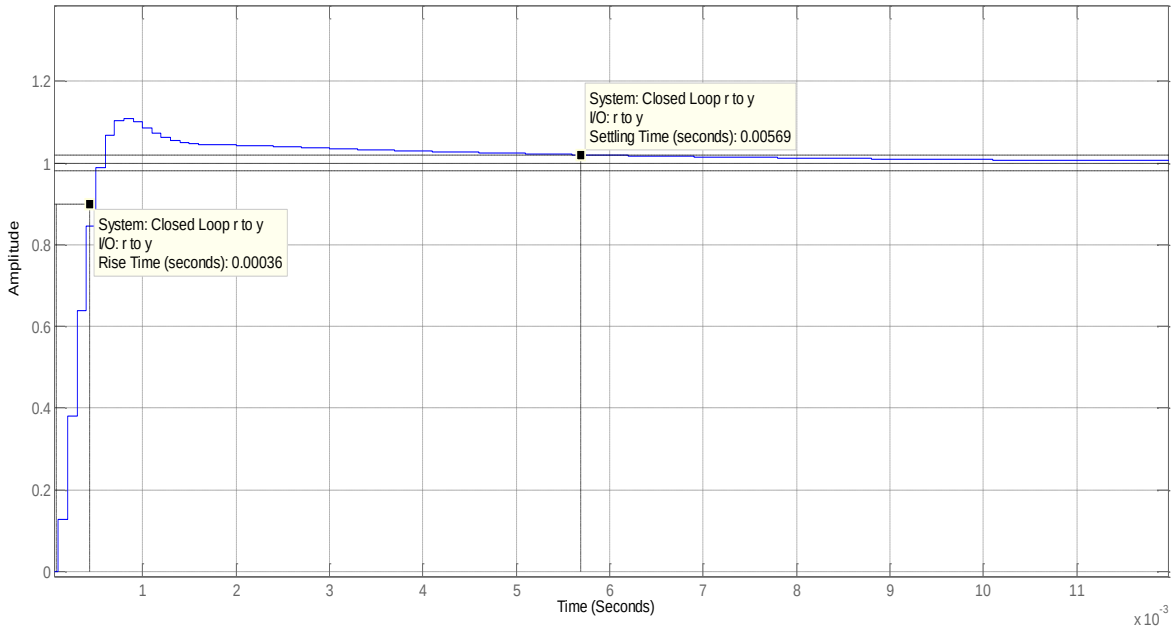


Figure 5.13: Load Side Voltage Loop Bode Plot and Step Response

The bode plot shows the gain margin of 16.7 *dB* and phase margin of 59.1° fulfilling the controller requirement. Rise time of 0.36ms and settling time of 5.6ms can also be observed in the above figure, indicating that the loop is stable.

5.4. Dual Vector Control using Sequence Separation

For unbalance voltage condition a negative dq sequence component appears in the rotating reference frame. The positive and negative sequence components can be separated using the method discussed in section 4.4.1. A control structure is then developed for the load side voltage control of the system and is illustrated in figure 5.14.

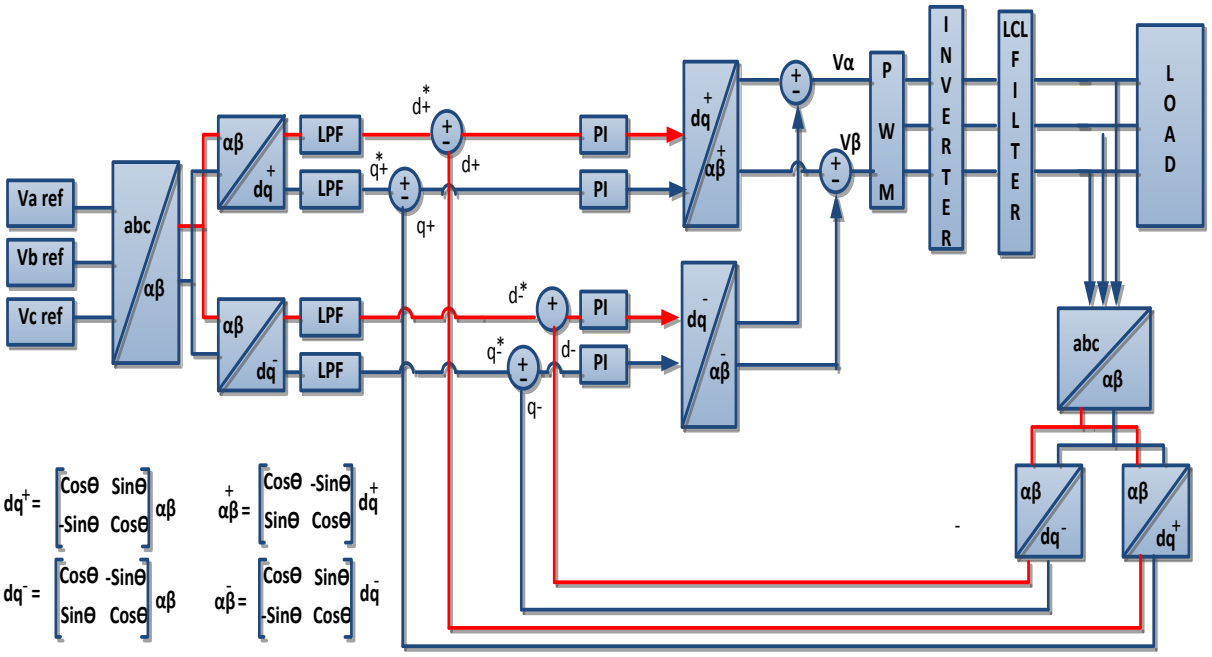


Figure 5.14: Dual Vector Control Structure for Load Side Control

The reference voltages for the positive and negative sequences are calculated using the sequence extraction method. The resulting error signals are passed through the PI controllers. Controller gain values are then applied. The signals for the converter reference voltages are then combined in the stationary reference frame as feedback and this is how the whole control works.

5.5. Conclusion

This chapter has presented a control structure of both sides of the system. Two tuning techniques were implemented to investigate the controller values for the control loops of each block. Pole zero maps were plotted to show the system stability. Frequency response analysis was also done with the help of bode and root locus plot. In the end dual vector control was discussed for the implementation of unbalanced voltage conditions.

CHAPTER 6

SIMULATIONS

All of the models that are to be implemented in the laboratory are first tested through simulations in the Labview environment with the help of Multism and the Simulation Interfacing Toolkit (SIT) which interfaces with MATLAB Simulink®. Interfacing Labview with Multisim is called co-simulation and its code structure is shown in Appendix B. Multisim is a strong analog and digital simulation software tool. With the help of co-simulation the entire system can be implemented in simulation before being prototyped. It makes it possible to design the entire real time system by checking the algorithms in Labview and connecting it to the hardware designed in Multisim. It serves as a powerful method with which to analyse design at an early stage. The simulations done were designed to represent the experimental setup as accurately as possible.

The main theme of this thesis is to develop a grid emulator for generating different voltage unbalances. A back-to-back converter topology has been used for controlled flow of bi-directional power, as discussed in earlier chapters. An in depth analysis and behavioural study of a two-level and a three-level converter connected in a back-to-back configuration is presented in figure 6.1. Detailed comparisons have been made on the basis of dynamic response and voltage magnitude deviation of the converters. The comparisons are shown with the help of simulations which are performed before the hardware implementation.

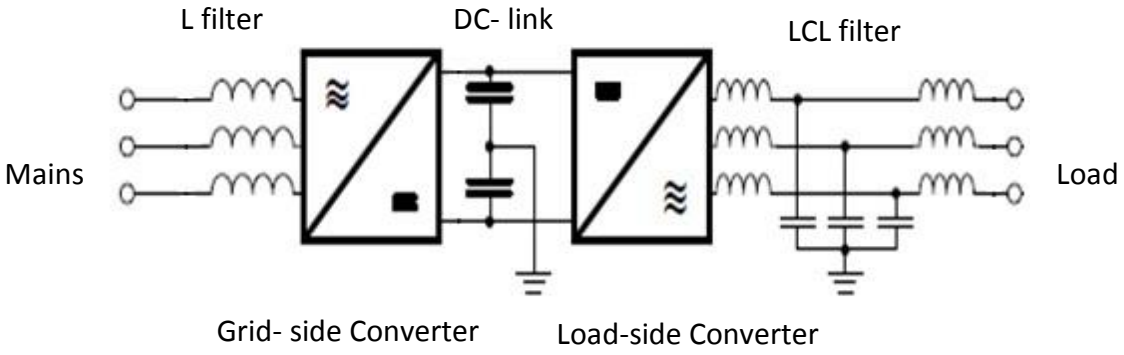


Figure 6.1: Back-to-Back Converters Configuration

With reference to figure 6.1 the structure of the system is explained. It can be seen that one converter is connected to the grid through an L filter. The other converter has a 30kW load attached to its output through an LCL filter. The switching frequency was set to 10kHz and the DC link nominal voltage was set to 800V for all the operations. Voltage oriented control was implemented with the current loop controller gains designed in chapter 5. For unbalanced conditions dual vector control was implemented. Positive and negative sequence components were extracted and manipulated to achieve stable control.

Complete system simulations with all components attached are analysed. Both converters are simulated for inversion (load side converter) and rectification (grid side converter) mode of operation by swapping their position in the layout. The grid side converter controls the DC link voltage and the load side converter performs as an inverter. There are two tests performed with the system. In the first test a three-level converter is tested on the grid side whilst a two-level converter is on the load side. In the second test a two-level converter is tested on the grid side whilst a three-level converter is on the load side.

Full system was simulated with both converters being connected in back-to-back configuration. For easy comparison between the two converter topologies the test results are shown in two complete sections named with the converter topology.

6.1. Two-level Converter

The two-level converter was first designed in Multisim at a component level. It was initially simulated as a grid-side converter (active rectification mode of operation) connected to the three-level converter on the load side. Then it was tested as a load-side converter (inverter mode of operation) connected to the three-level converter on the grid side. The SVPWM technique was used to control the converters as discussed in chapter 3. The PWM switching signals developed in the Labview environment, which was then applied to the converter within Multisim, and the output waveforms were analysed in a Labview scope window.

6.1.1. PWM Switching Signals of the Two-Level Converter

Line-to-line PWM waveforms are shown in figure 6.2. The filtered line-to-line PWM waveforms which show the fundamental line-to-line waveforms are also shown. In this chapter all the simulations are done for line-to-line converter voltages.

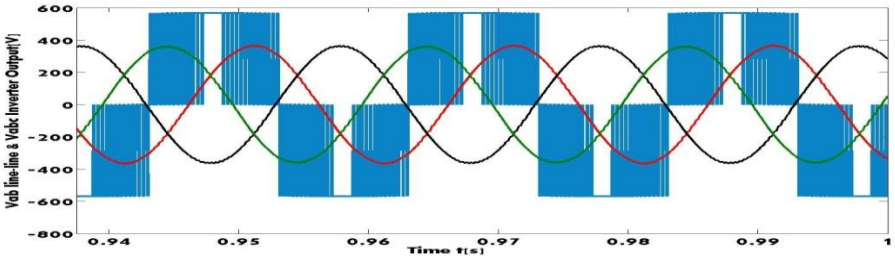


Figure 6.2: Vab line-line Before Filtering and Vabc Output Voltage

6.1.2. Active Rectification Mode of Operation

The two-level converter was simulated as a grid-side converter to control the DC link voltage. This operating mode is also called active rectification. The main features of the active rectifier are:

- Bi-directional power flow.
- Sinusoidal input current.
- Regulation of input power factor.
- Low total harmonic distortion of the input current.
- Controlled DC link voltage

A voltage oriented control was applied with the aid of PWM to achieve a stable DC link voltage in active rectifier mode of operation. The rectification portion which was simulated is shown in figure 6.3.

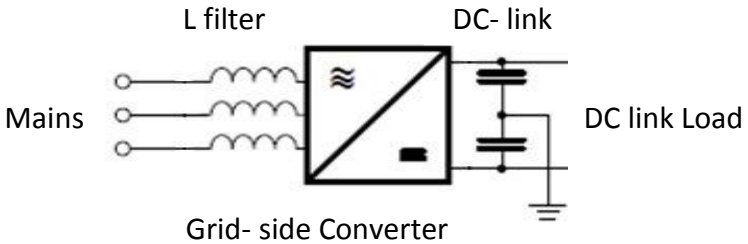


Figure 6.3: Grid-Side Converter as Active Rectifier

The dynamic response of the two-level converter in rectifier mode was analyzed. The DC link voltage set-point was changed from 300 V to 150 V and then back to 300 V in this test. A change in DC voltage results in proportional change to the output current. The simultaneous change in voltage and current was done to verify the closed loop stability of the control system.

Figure 6.4 presents a steady state flow of the DC link voltage and the dynamic response of the converter. Dynamic response can be assessed by introducing a step in its value. When the set point was changed from 300 V to 150 V, figure 6.4 indicates a settling time of 50ms and its recovery time is 30ms.

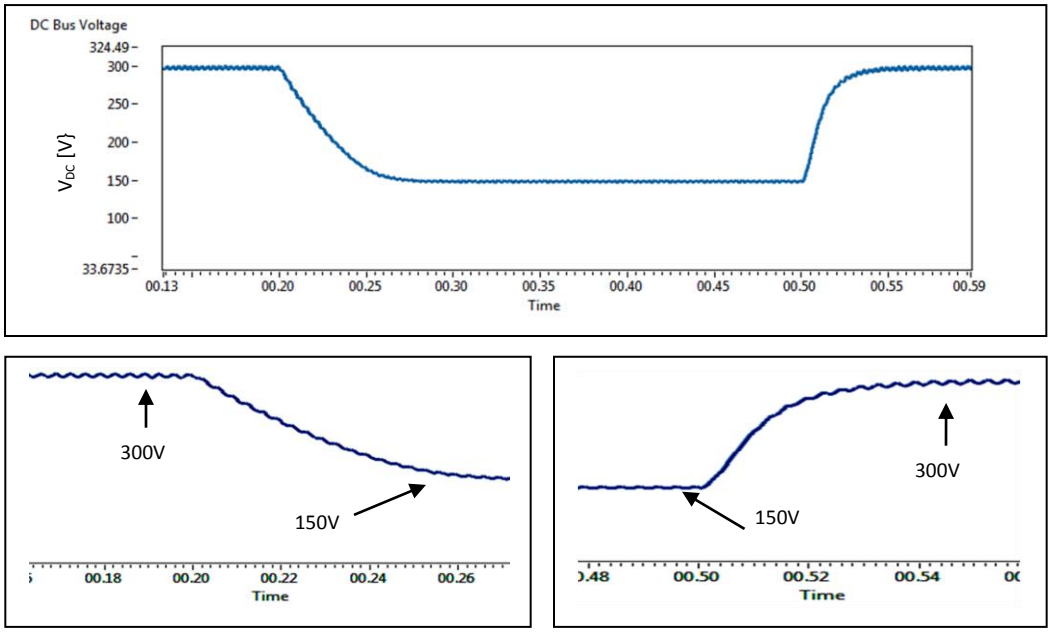


Figure 6.4: DC Link Voltage Step

The effect on input grid current is shown in figure 6.5. The inductors on the input of the converter reduce the switching ripple and ensure sinusoidal grid current. The change in the grid currents can be seen on the same instances when the DC link voltage step was applied. When a DC voltage step was applied a non-zero value of reactive power appeared. But this reactive component only appears for a few μs during transient. For constant impedance load across the DC link, the drop in V_{dc} should correspond to a boost in current on the grid side.

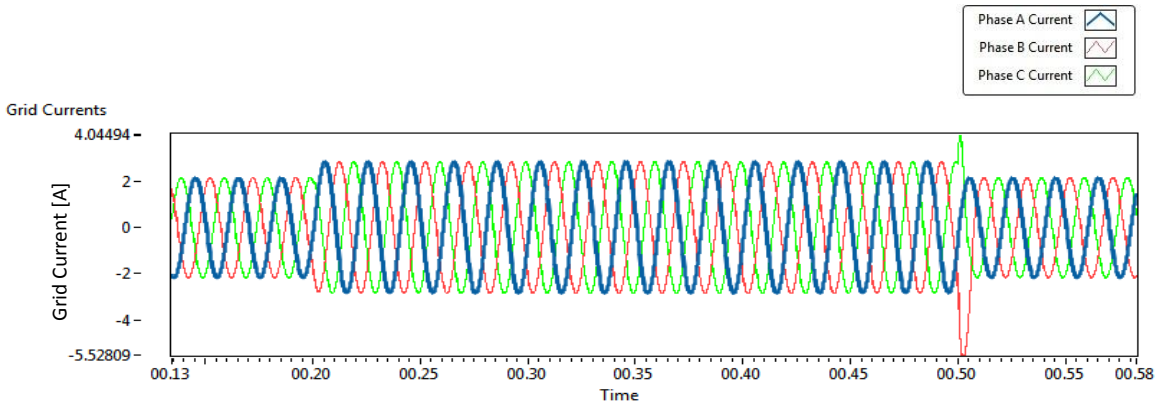


Figure 6.5: Grid Current Affected by DC Link Voltage Step

6.1.3. Inverter Mode of Operation

The two-level converter is then operated in inverter mode connected to the DC link controlled by the three-level converter. This will be further analysed in subsequent sections. As mentioned earlier, the main objective of this thesis is to produce different voltage variations on the output of the grid emulator connected to a load. A 30kW load is considered here for the simulations. The voltage should be regulated according to the unbalance created. Inverter mode setup is shown in the figure below.

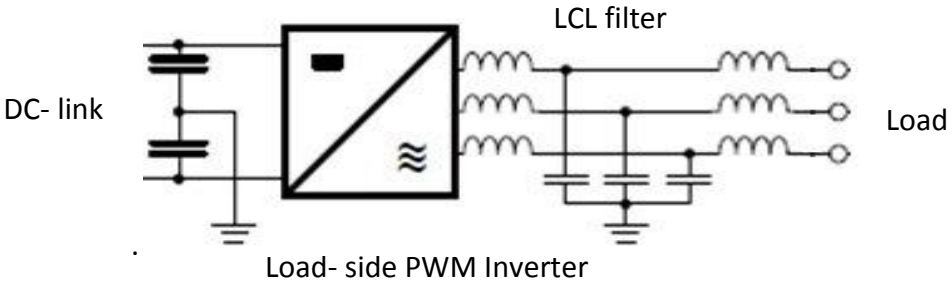


Figure 6.6: Load-Side Converter in Inverter Mode

As discussed in chapter 2 the voltage unbalance could be of various types. Unbalance on a single phase occurs when an unbalanced load is connected to it. The voltage unbalances implemented in this thesis are under-voltage (dip) and over-voltage (swell). These unbalances occur as a result of disturbances on one or more phases.

6.1.3.1. Voltage Sag/Voltage Dips

Voltage dips occur as a result of decrease of the normal voltage level between 10% and 90% of the nominal rms voltage on one or more phases for durations of 0.5 cycles to 1 minute. In this thesis only the magnitude unbalance of this type is implemented. In particular type A,B and E dips will be considered. Dual vector control was implemented to control in order to implement the dip on each phase and hence the intended unbalance was created. Different loads were then used to check the steady voltage regulation. For simulations a 30kW resistive load was considered.

- **Type A Dip**

  Type A was introduced by changing the Va, Vb and Vc reference values as discussed in figure 5.14. This reduces the magnitude on all three phases. The phase angles are maintained thereby allowing symmetrical magnitude change to be implemented as shown in figure 6.7.

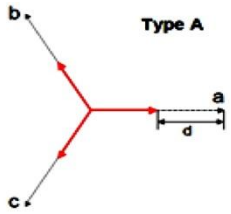


Figure 6.7: Type A Voltage

Figure 6.8 shows the output voltage waveform where change in magnitude on all three phases can be seen.

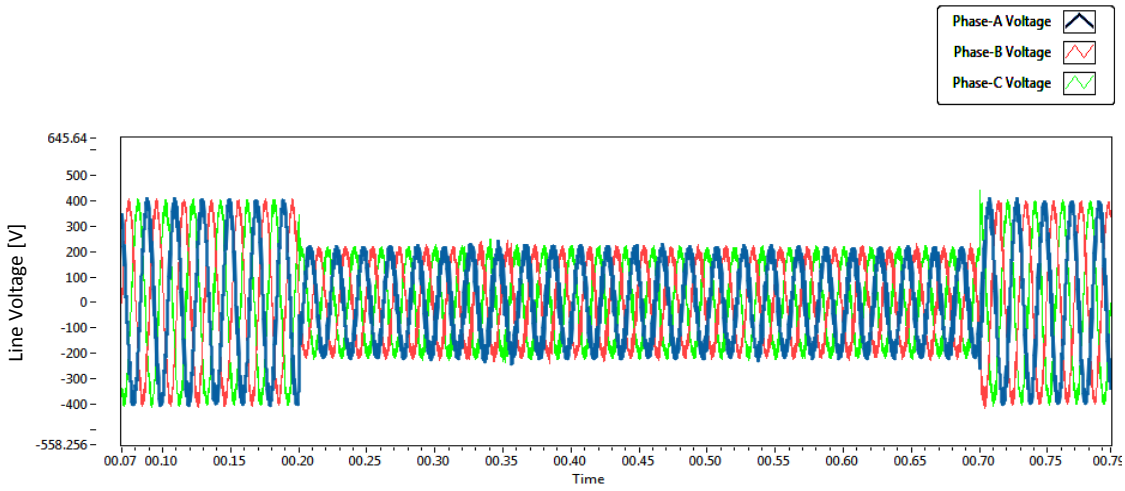


Figure 6.8: Type A Dip implemented

A 50% voltage dip was implemented for 0.5 seconds. Zoomed-in screen shots are shown below in figure 6.9 illustrating the dip shape and its start time.

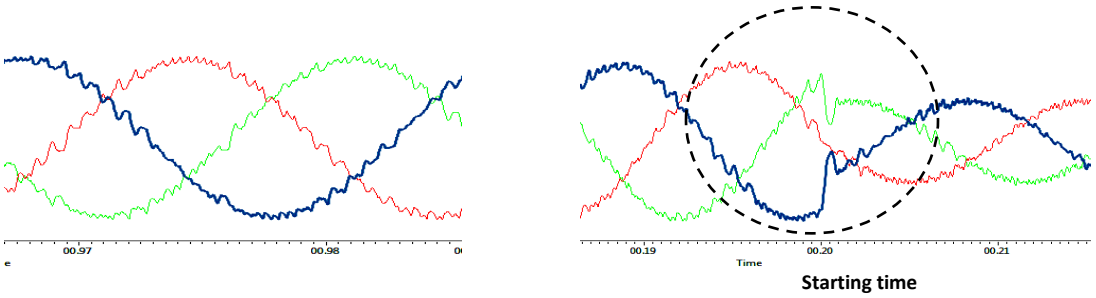


Figure 6.9: Zoomed-in Screen Shots of the Dip Implemented

For the analysis of the converters dynamic response, the three phase voltages are converted into *dq* components. As Type A is a symmetrical dip, there will be no negative sequence component in this sequence case and has a zero quadrature axis component. Positive *dq* waveforms are shown in figure 6.10.

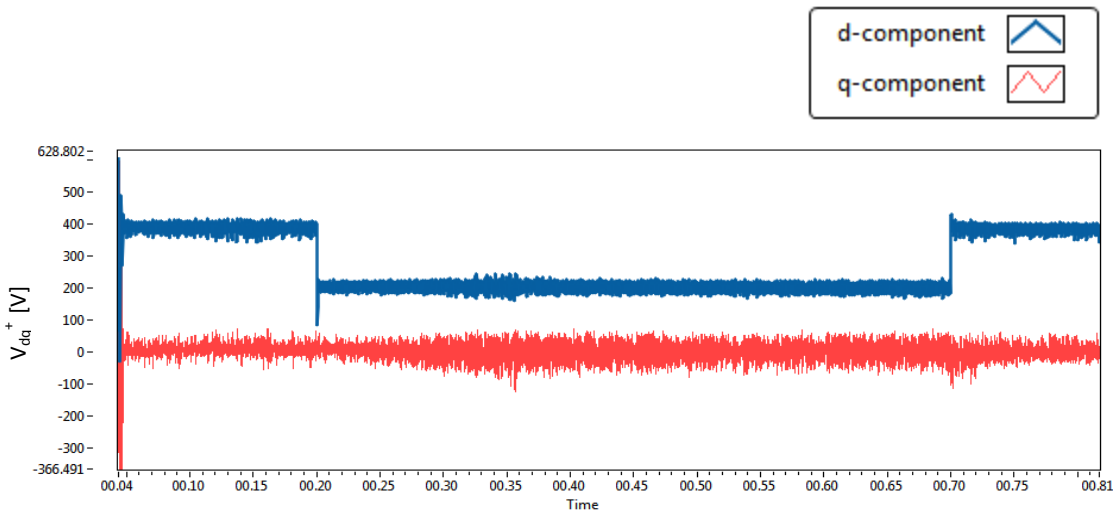


Figure 6.10: Positive dq Components of the Type A Dip Implemented

Zoomed-in screen shots of the *d*-component in the above figure are shown below

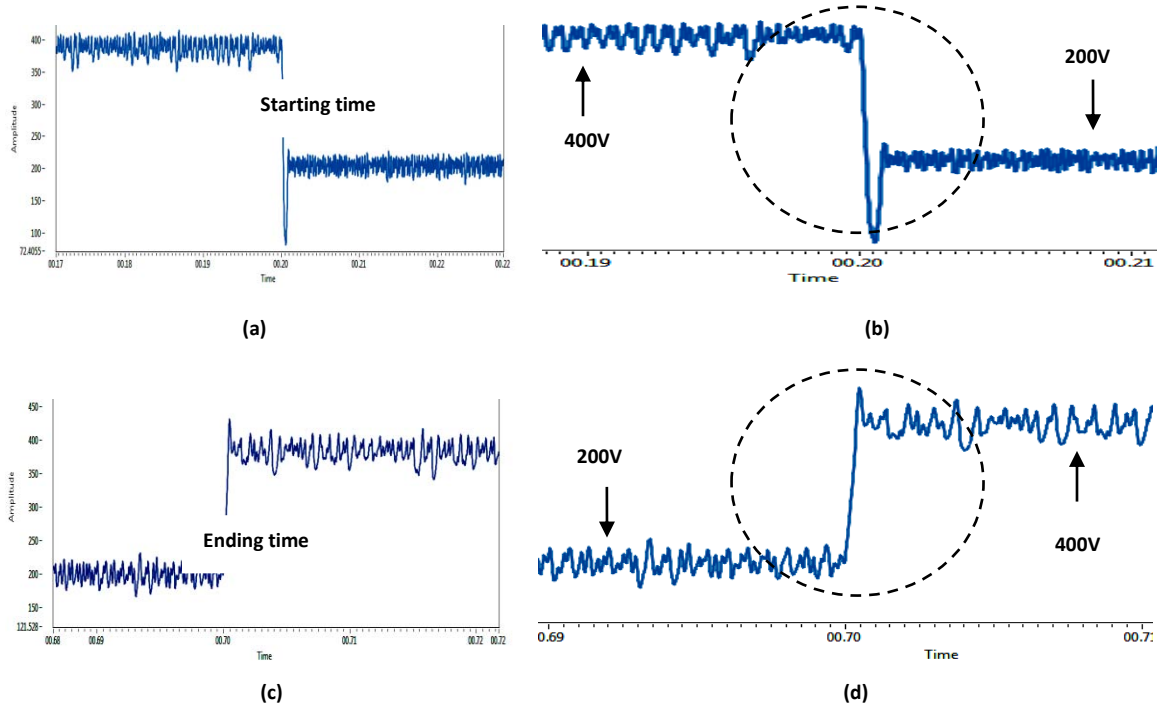


Figure 6.11: Zoomed-in Screen Shots of the d Component for Type A Dip

Figure 6.11 (b) and (d) show the settling time of 1ms for the dip. Detailed dynamic response analysis is presented in chapter 8 where comparisons are based on experimental results.

➢ Type B Dip

Type B dip was introduced to the system by again changing the voltage reference values. It reduces the magnitude on one phase while maintaining the other two at nominal value. The phase angles are maintained thereby allowing magnitude unbalance to be implemented as shown in figure 6.12.

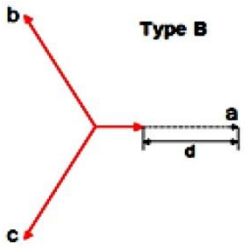


Figure 6.12: Type B Voltage Dip

Figure 6.13 shows the waveforms in which a single phase has a lower magnitude and the other two phases remain on the nominal value without phase unbalance.

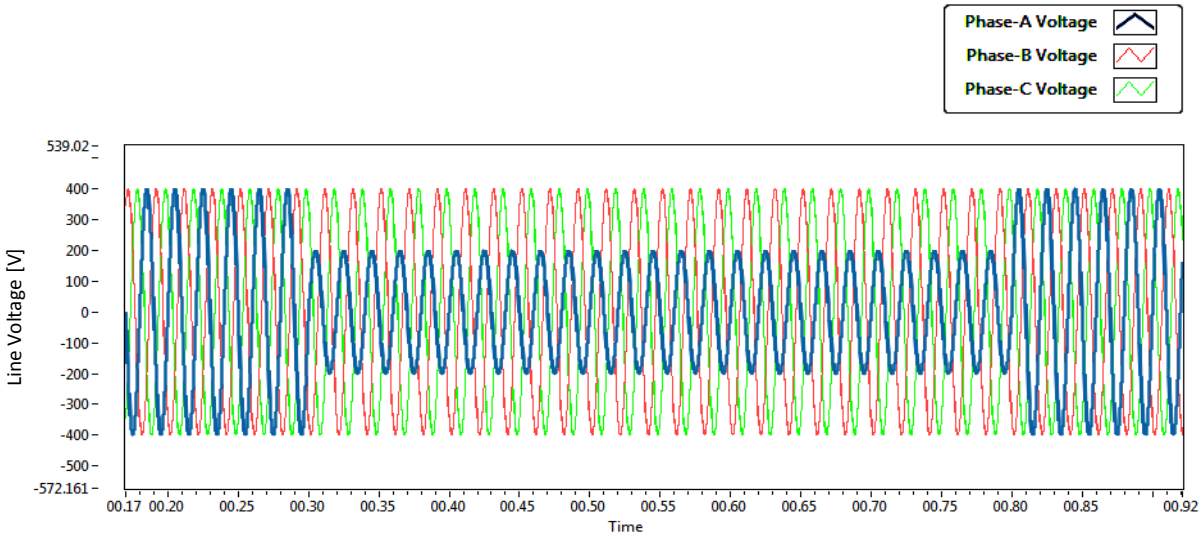
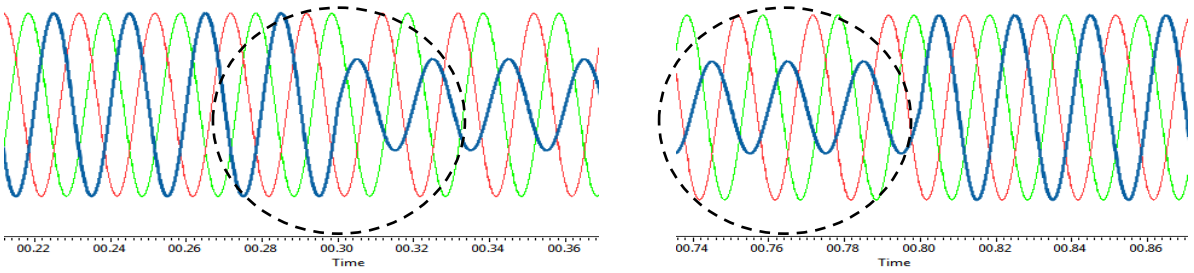


Figure 6.13: Type B Dip Implemented

A 50% voltage dip was implemented on phase-A for 0.5 seconds. Zoomed-in screen shots are shown below in figure 6.14 illustrating the start and end of the dip implemented.



Start time **End time**

Figure 6.14: Zoomed-in Screen Shots of the Dip Implemented

Three phase voltages are then converted into *dq* components. As this is an unsymmetrical dip, a negative sequence component also appears in the *dq* reference frame. Dual vector control explained in chapter 5 was then applied to control the negative sequence voltage. Figure 6.14 and 6.15 show the positive and negative sequence *dq* voltages under the unbalanced condition. Dual vector control can be used to force the negative sequence voltages to zero thereby restoring the positive sequence voltages to their original values and hence acquiring balanced conditions. However in the case of the grid emulator, negative sequence components are not suppressed, since voltage unbalance is intentionally created to test the behaviour of the system connected to the emulator. The controller performed as expected for the required unbalanced set points.

The settling time of unbalance is almost 1ms. In this thesis comparison is made between percentage magnitude deviation and the waveform distortion. According to the IEC power quality standards there are two main characteristics of the voltage dips : “residual voltage” and “duration”. Residual voltage is the minimum rms voltage recorded within the voltage dip which lies above or below the dip magnitude threshold [43]. The Difference between the dip threshold value and the residual voltage value can be called magnitude deviation.

In this thesis a comparison is made between the two converter topologies on the basis of percentage magnitude deviation with respect to the symmetrical voltage dip threshold value, and is shown in figure 6.15. Rotating reference fame components *‘d‘* and *‘q’* were calculated from the output load voltage by using transformation equations 4.17 & 4.18. For an

unsymmetrical dip a change in the *dq* components values was expected and is related to the residual voltage scenario as discussed above.

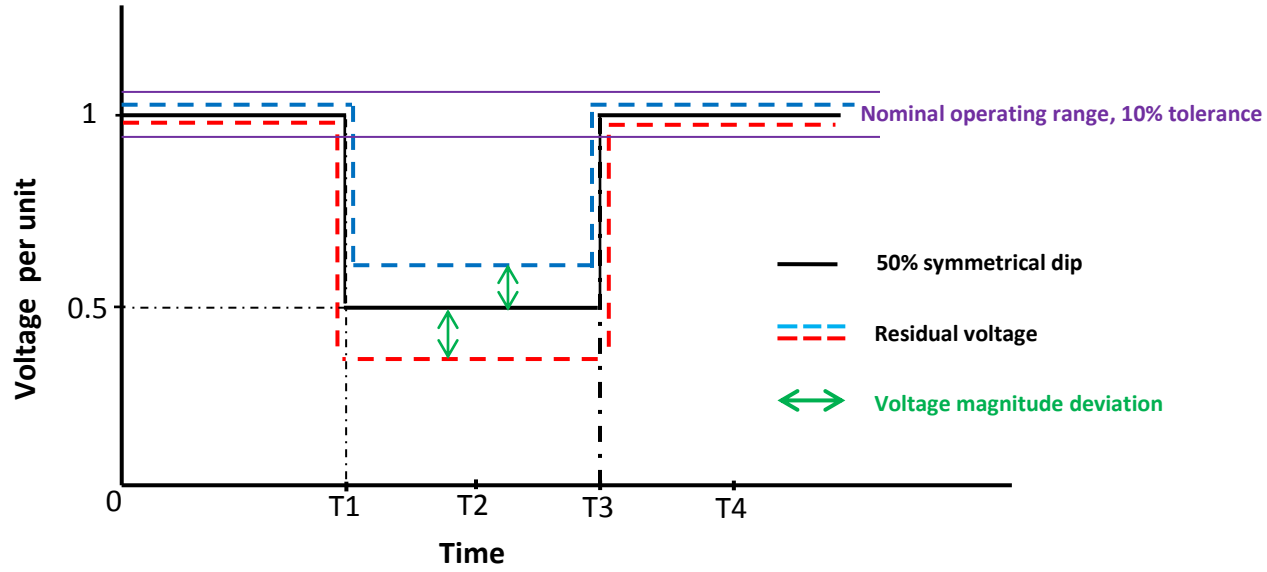


Figure 6.15: Symmetrical dip and Residual Voltage Graph

Figure 6.16 shows positive sequence components of Type B dip. A 50% dip on one phase was applied for 0.5 seconds which led to a 30% magnitude deviation. For a 50% symmetrical voltage dip the waveform should go to the half of the peak voltage i.e 200V but here the positive sequence *d*-component only went down to 320V which is the residual voltage, thereby generating 120V of magnitude deviation whereas the *q*-component stayed at zero.

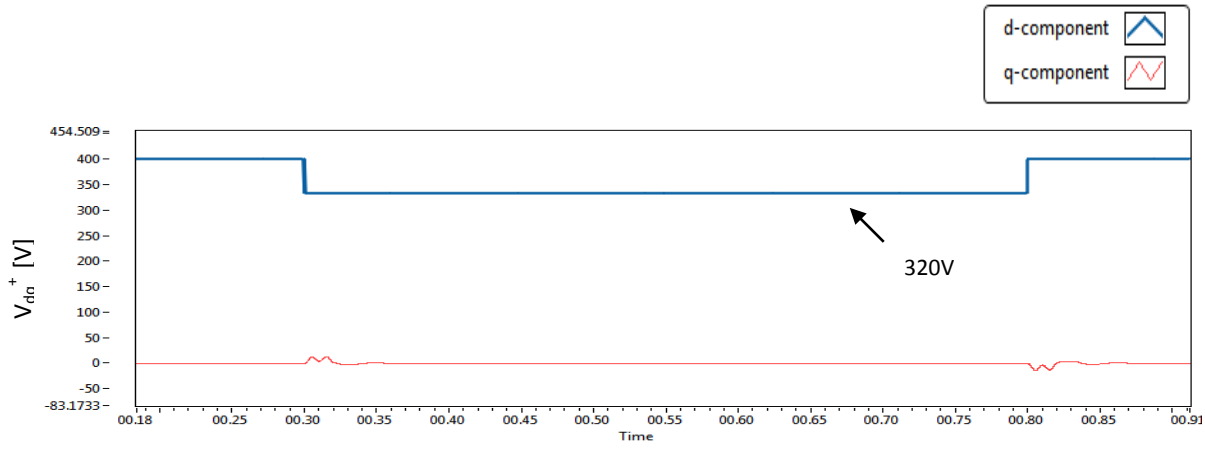


Figure 6.16: Positive *dq* Components of the Type B Dip Implemented

Similarly in figure 6.17 the negative *d*-component for symmetrical dip condition should stay at zero but here it touches 30V which is the residual voltage itself. Thereby generating 7.5% of magnitude deviation and *q*-component stays at zero respectively.

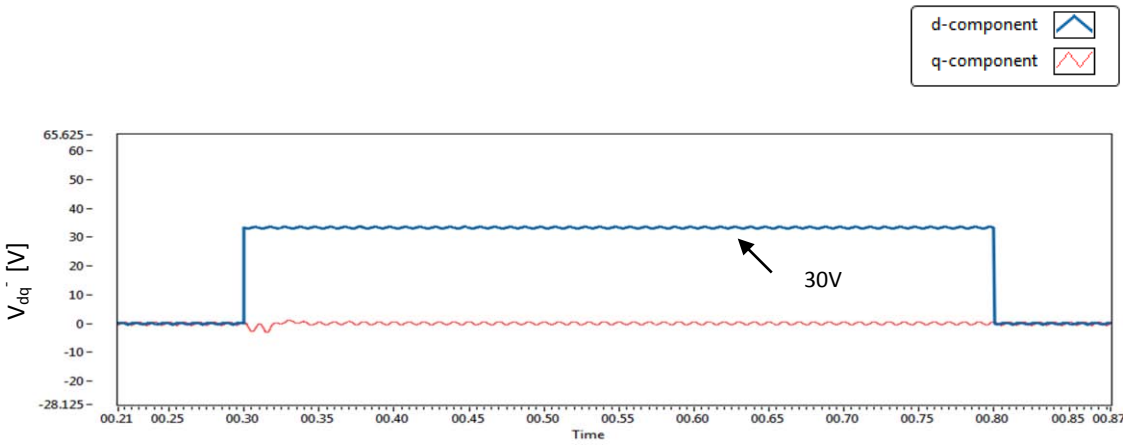


Figure 6.17: Negative *dq* Components of the Type B Dip Implemented

➢ Type E Dip

This dip reduces the magnitude on two phases while maintaining the third at nominal voltage. The phase angles are maintained thereby allowing magnitude unbalance to be implemented as shown in figure 6.18.

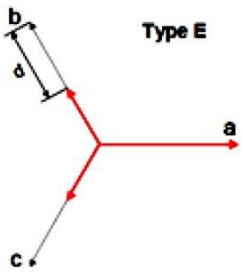


Figure 6.18: Type E Voltage Dip

Figure 6.19 shows the waveform in which two phases have low magnitude.

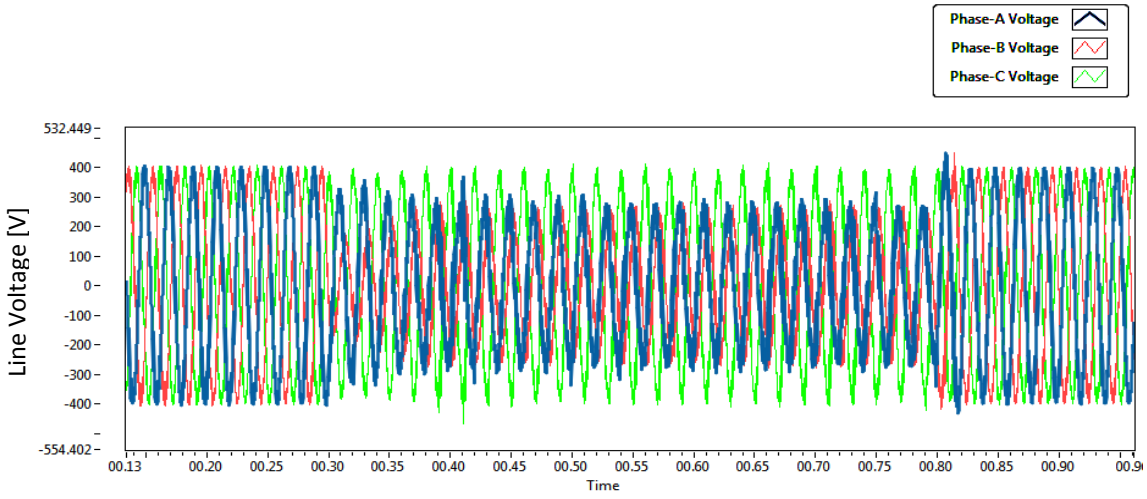
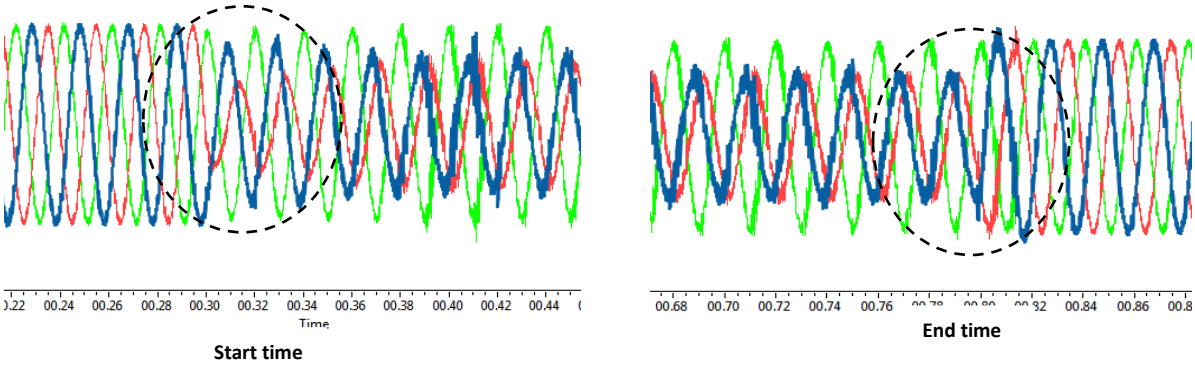


Figure 6.19: Type E Dip Implemented

A 50% voltage dip was implemented on phase-A and B. Zoomed-in screen shots are shown below in figure 6.20 illustrating the start and end of the dip implemented.



Start time

End time

Figure 6.20: Zoomed-in Screen Shots of the Dip Implemented

Three phase voltages are then converted into *dq* components. Figure 6.21 and 6.22 show the positive and negative sequence *dq* voltages under unbalance condition. Figure 6.21 illustrates *dq*-positive sequence components. A 50% dip was applied which resulted in 15% magnitude deviation. Here the positive *d*-component went down to almost 260V which is the residual voltage with 60V of magnitude deviation whereas the *q*-component stayed at zero. A transient was also seen in the beginning and at the end of the dip for less than 0.1s. Moreover, it was

noticed from the figure 6.16 and 6.21 that the positive *d*-component in the Type-E dip had lower magnitude deviation than the Type-B. From the results it was investigated to be 15%.

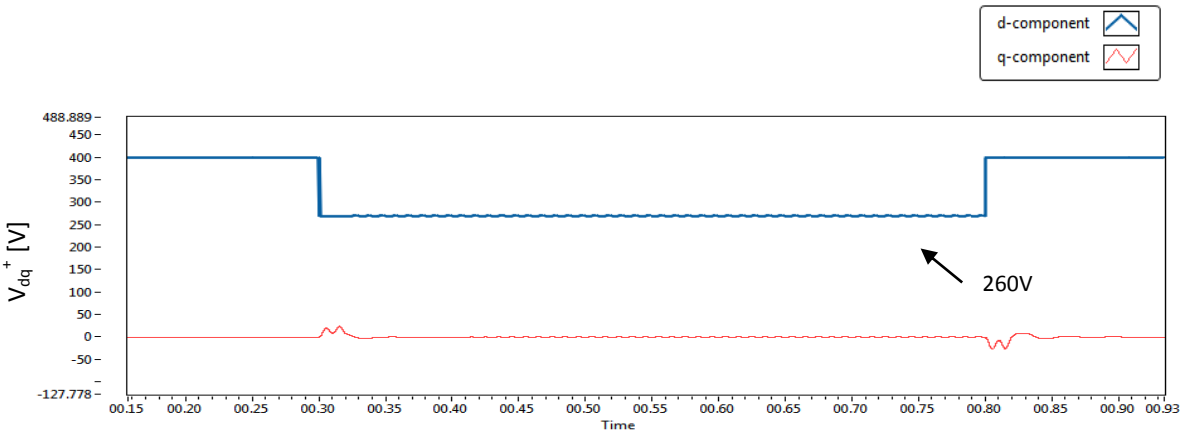


Figure 6.21: Positive *dq* Components of the Type E Dip Implemented

Similarly in figure 6.22, the negative *d*-component has 10% magnitude deviation with -40V of residual voltage and *q*-component stayed at zero. In addition to this, a Type-E dip has a higher negative *d*-component deviation than the Type-B dip. The negative value for the d component was expected from the voltage transformation equations.

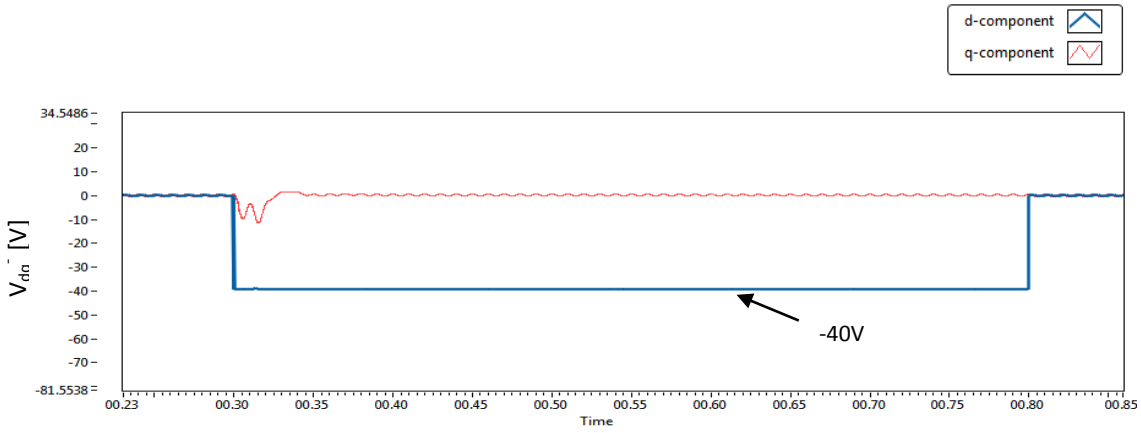


Figure 6.22: Negative *dq* Components of the Type E Dip Implemented

6.1.3.2. Voltage Swell/Overvoltage

This is a momentary increase of the voltage, at the power frequency, outside the normal tolerances, with duration of more than one cycle and typically less than a few seconds. In the

figure below a 50% symmetrical overvoltage is implemented.

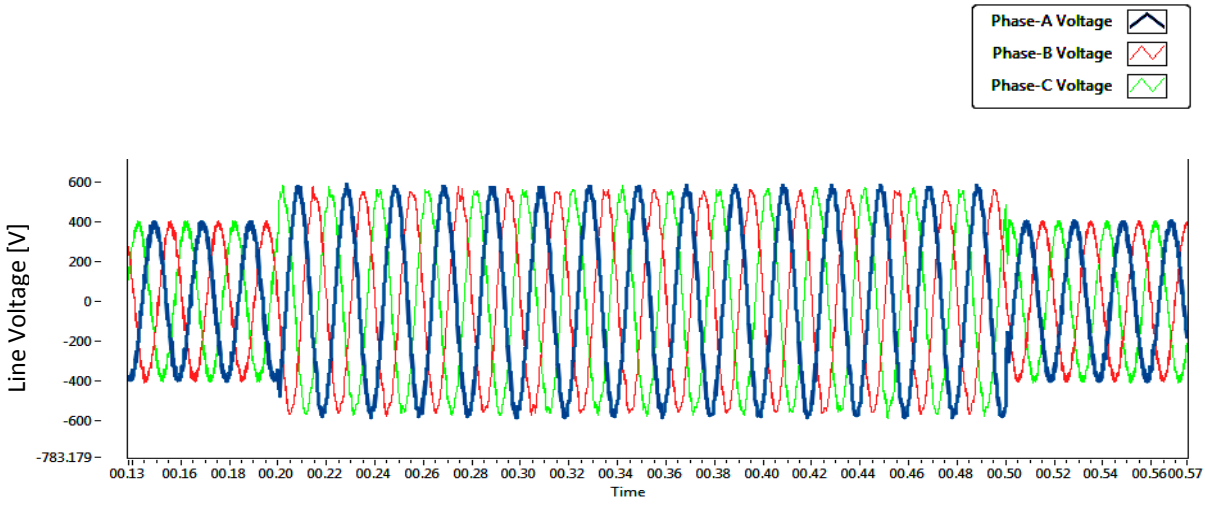


Figure 6.23: Symmetrical Overvoltage Implemented

A 50% overvoltage was implemented on all three phases. Zoomed-in screen shots are shown below in figure 6.24 illustrating the start and end of the overvoltage implemented.

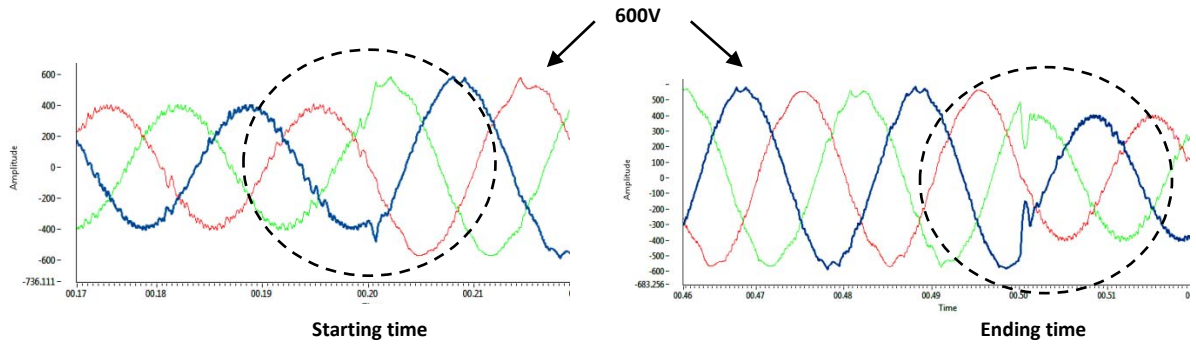


Figure 6.24: Zoomed-in Screen Shots of the Overvoltage Implemented

For the dynamic response analysis the three phase voltages are converted into *dq* components. As it is a symmetrical overvoltage, there will be no negative sequence component hence positive *dq* waveforms are shown in figure 6.25.

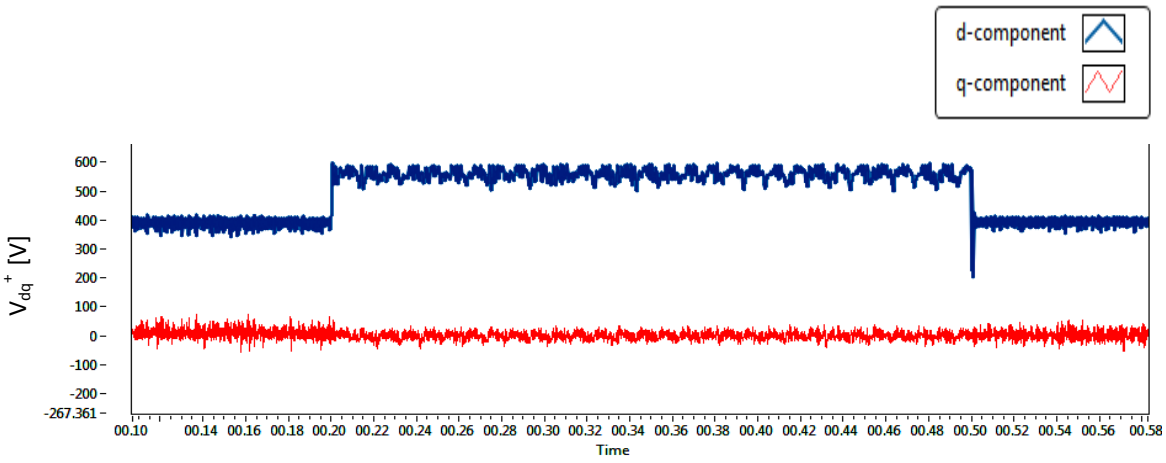


Figure 6.25: Positive *dq* Components of the Symmetrical Overvoltage Implemented

Zoomed-in screen shots for the start and end of the overvoltage are shown below. Figure 6.26 depicts the settling time of the overvoltage and i.e almost 1ms.

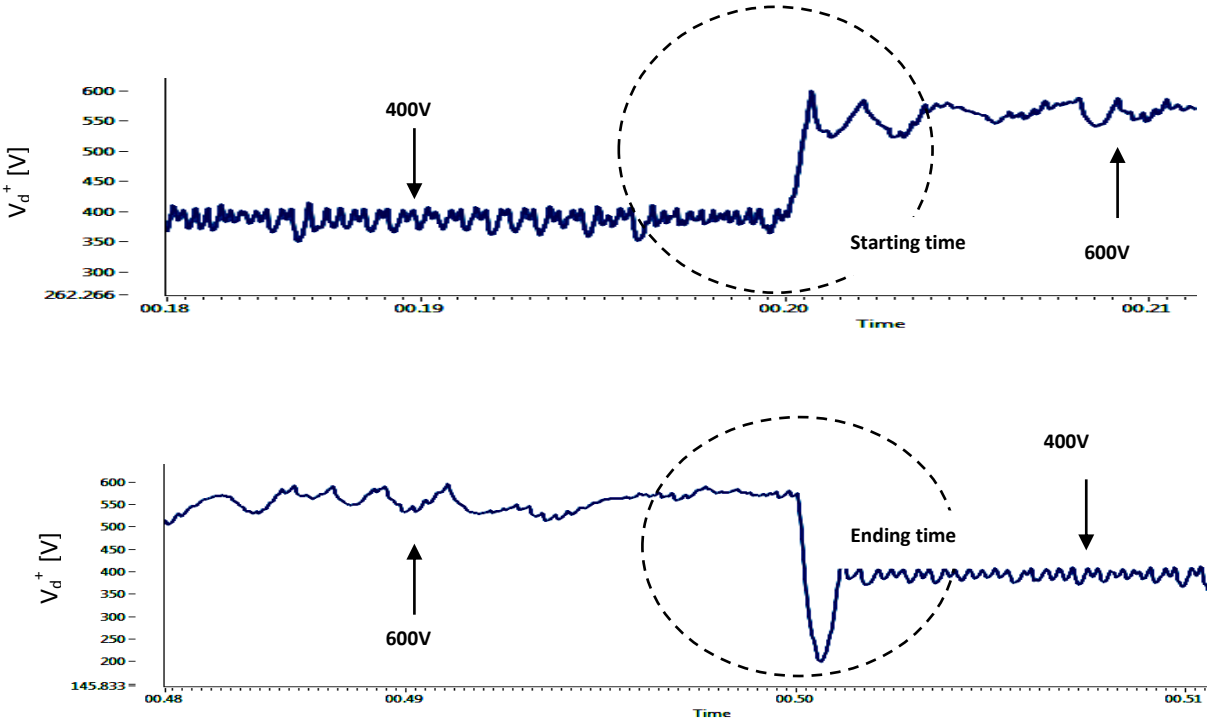


Figure 6.26: Zoomed-in Screen Shots of the *d* Component

6.2. Three-level Converter

The three-level converter is simulated and analysed in this section. The same procedure is followed as section 6.1 in order to compare both converters. A three-level converter was initially simulated as a grid-side converter (in rectifier mode of operation) connected to the two-level converter on the load side. After that it was simulated as a load-side converter (in inverter mode operation) connected to the two-level converter on grid side. The switching signals developed in Labview were then applied to the converter switches within the Multisim environment. The output waveforms and the dynamic responses were then analysed in Labview scope windows.

6.2.1. PWM Switching Signals of the Three-Level Converter

Simulation model for a three-level converter was implemented as shown in Appendix-B. A line-to-line PWM waveforms are shown in figure 6.27. The filtered line-to-line PWM waveforms which show the fundamental line-to-line waveforms are also shown. Three levels of the voltage steps can be seen as discussed in chapter 3. The purpose is to generate the required PWM waveform for performing the converter functions.

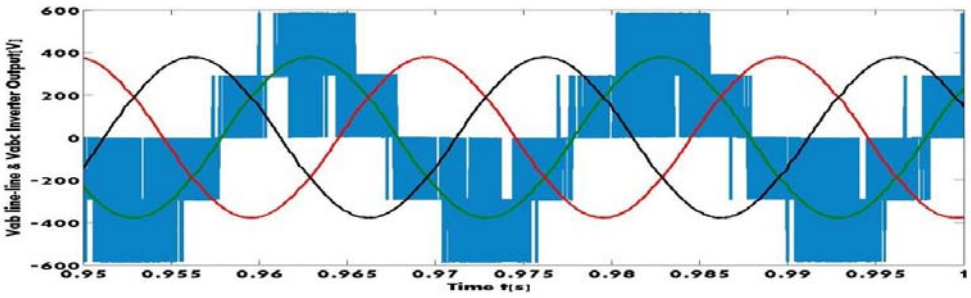


Figure 6.27: Vab line-line Before Filtering and Vabc Output Voltage

6.2.2. Active Rectification Mode of Operation

A three-level converter was simulated as a grid-side converter to control the DC link voltage. A voltage oriented control was applied with the help of PWM to get the stable DC link voltage for inverter operation.

The dynamic response of the three-level converter in rectifier mode was analysed. The DC link voltage set-point was changed from 310V to 130V and then back to 310V in this test. A change in DC voltage results in proportional change to the output current. The simultaneous change in voltage and current was done to verify the closed loop stability of the control system. The figure below presents a steady state and dynamic response of the converter. When the set point was changed from 310V to 130V, figure 6.28 indicates settling time of 30ms and on its recovery time is 25ms.

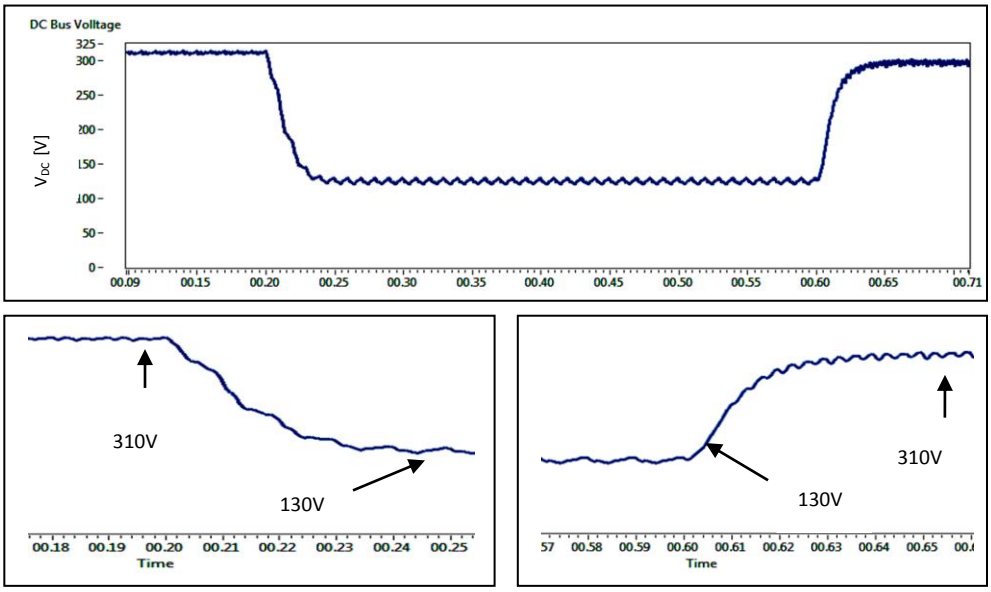


Figure 6.28: DC Link Voltage Step

Effect on input grid current is shown in figure 6.29. Change in the grid currents can be seen on the same instances when DC link voltage step was applied. For constant impedance load across the DC link, the drop in V_{DC} should correspond to a slight boost in current on the grid side which depends on the controller gains and the feedback.

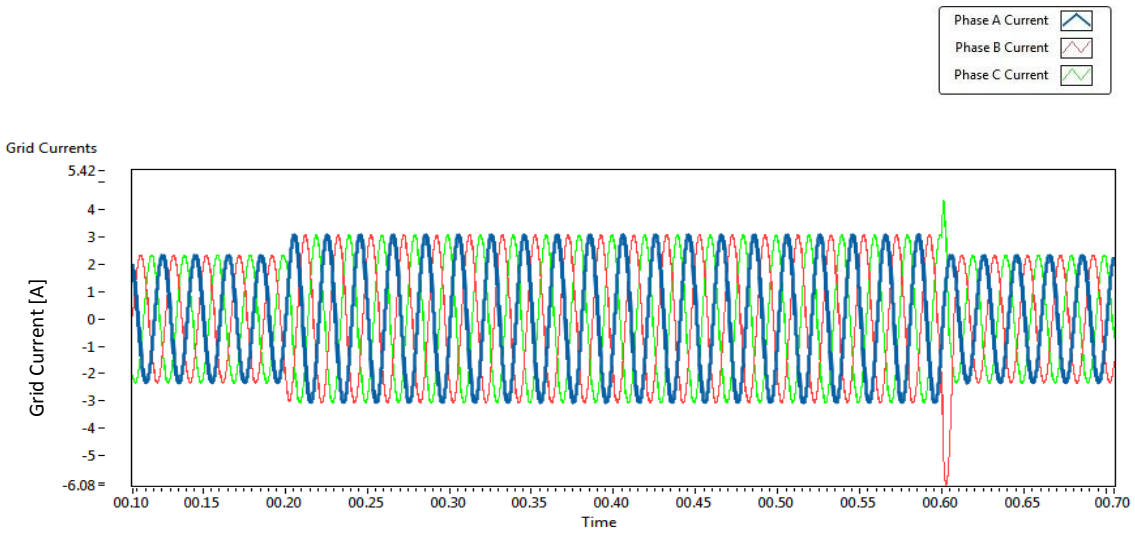


Figure 6.29: Grid Current Affected by DC Link Voltage Step

It is to be noted from figures 6.5 and 6.28 that the three-level converter step response for the DC link voltage is bit faster and with less distortion as compared to the two-level converter.

6.2.3. Inverter Mode of Operation

In this section the three-level converter is operated in inverter mode of operation connected to the two-level converter on the grid side as shown in figure 6.1. As mentioned earlier the main objective of this thesis is to produce different voltage variations on the output of the grid emulator regardless to the load connected to it. The same load is used as shown in figure 6.6. The voltage unbalances implemented in this thesis are under-voltage (dip) and over-voltage (swell). These unbalances occur as a result of disturbances on one or more phases.

6.2.3.1. Voltage Sag/Voltage Dips

Type A, B and E dips are investigated for the three-level converter. Dual vector control was implemented to control each phase and dips were generated considering balanced grid condition.

- **Type A Dip**

  Type A was introduced to the system as discussed in section 6.1.4. It reduces the magnitude on all three phases. The phase angles are maintained thereby allowing symmetrical

magnitude unbalance to be implemented. Figure 6.30 shows output voltage waveform where change in magnitude on all three phases can be seen.

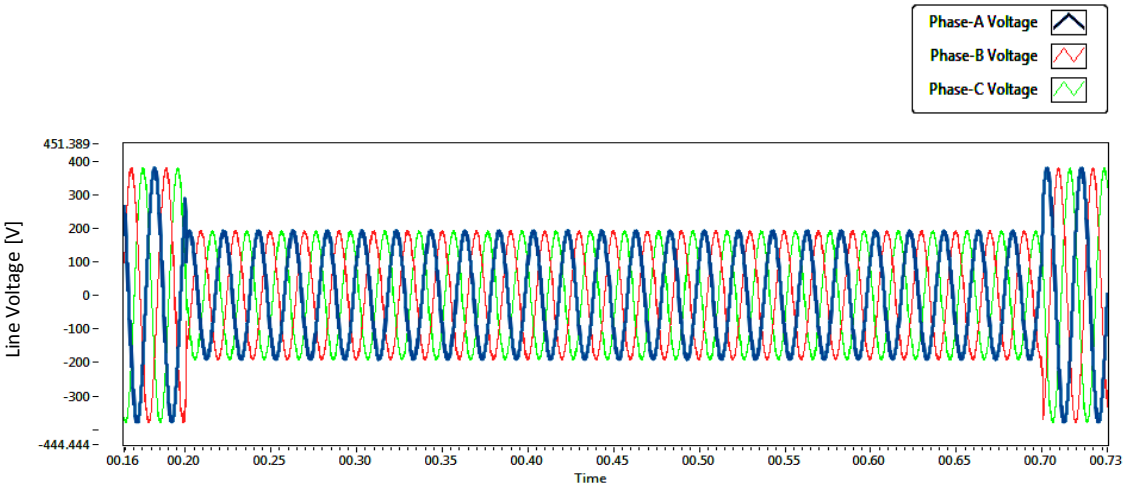
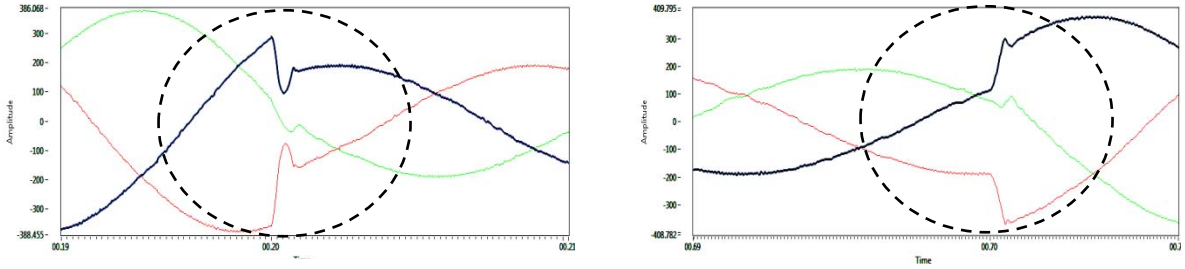


Figure 6.30: Type A Dip Implemented

A 50% voltage dip was implemented for 0.5 seconds. Zoomed-in screen shots are shown below in figure 6.31 illustrating the dip shape with its start and end time.



Start time **End time**

Figure 6.31: Zoomed-in Screen Shots of the Dip Implemented

By comparing figures 6.9 to figure 6.31 It can be seen that the output waveform of the three-level converter is much smoother than that of the two-level converter which was expected from the discussion in chapter 2 and 3. Now for proper dynamic response analysis the three phase voltages are converted into *dq* components. As Type A is a symmetrical dip, there will be no negative sequence component in this sequence case. Positive *dq* waveforms are shown in figure 6.32.

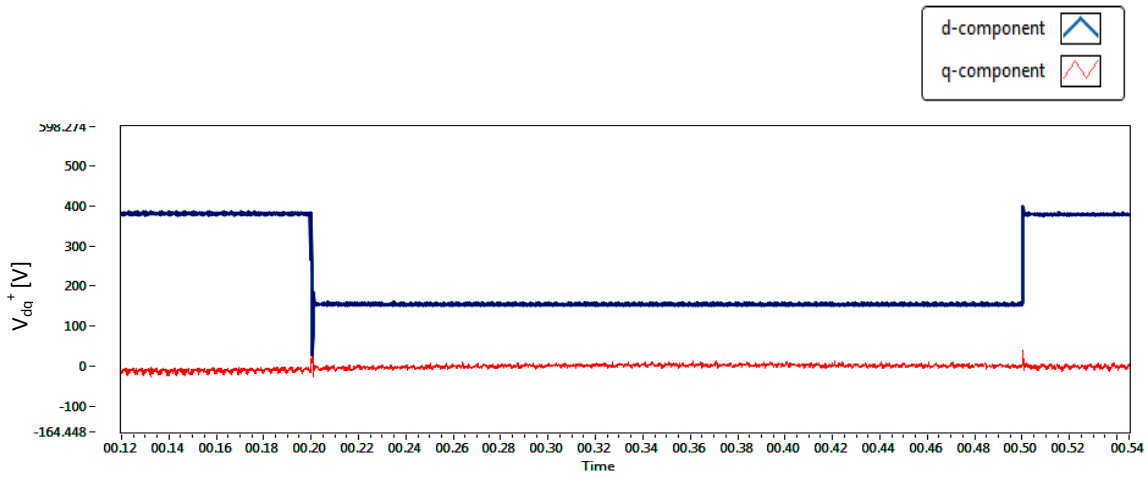
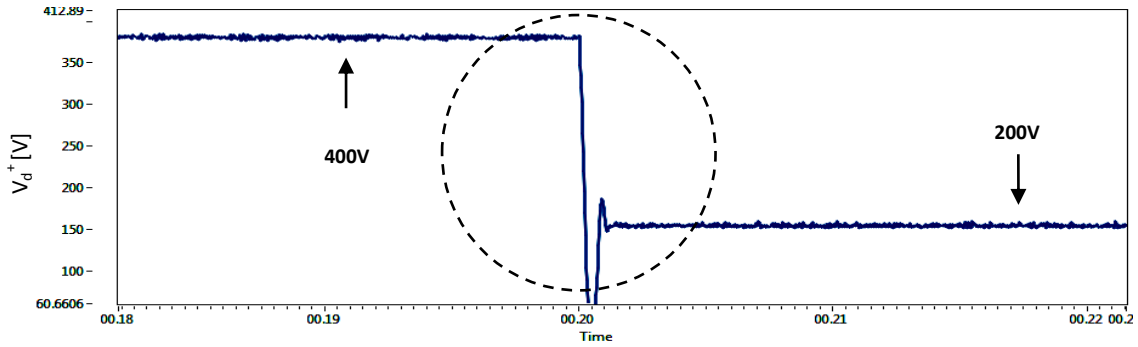
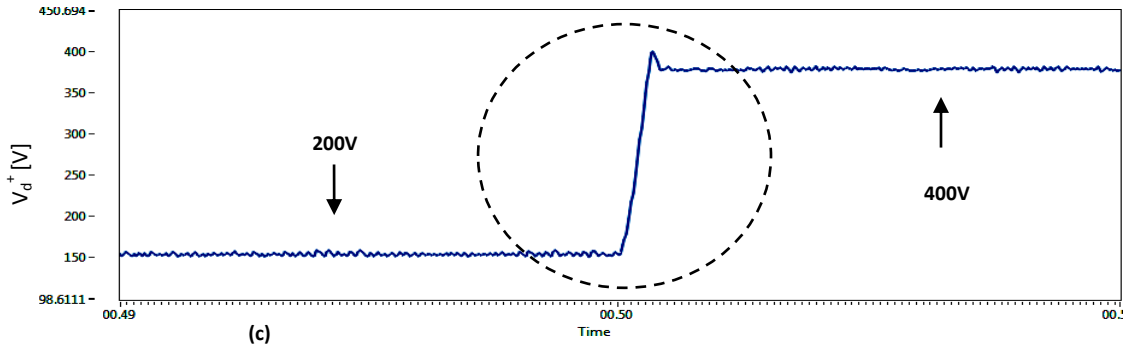


Figure 6.32: Positive *dq* Components of the Type A Dip Implemented

Zoomed-in screen shots for positive d-component are shown below



(a) Start time of the dip



(c)

(b) End time of the dip

Figure 6.33: Zoomed-in Screen Shots of the *d* Component for Type A Dip

Figure 6.33 shows the settling time taken by the dip and i.e almost 1ms. Lower ripple level of *Vd* and *Vq* in figure 6.33 can be seen as compared to figure 6.11 which confirms the THD discussion in chapter 3. Proper dynamic response analysis is done in chapter 8 where all the comparisons are concluded on experimental basis.

➢ Type B Dip

Type B was introduced to the system. It reduces the magnitude on one phase while maintaining the other two at nominal value. The phase angles are maintained thereby allowing magnitude unbalance to be implemented. Figure 6.34 shows the waveform in which a single phase with less magnitude can be seen.

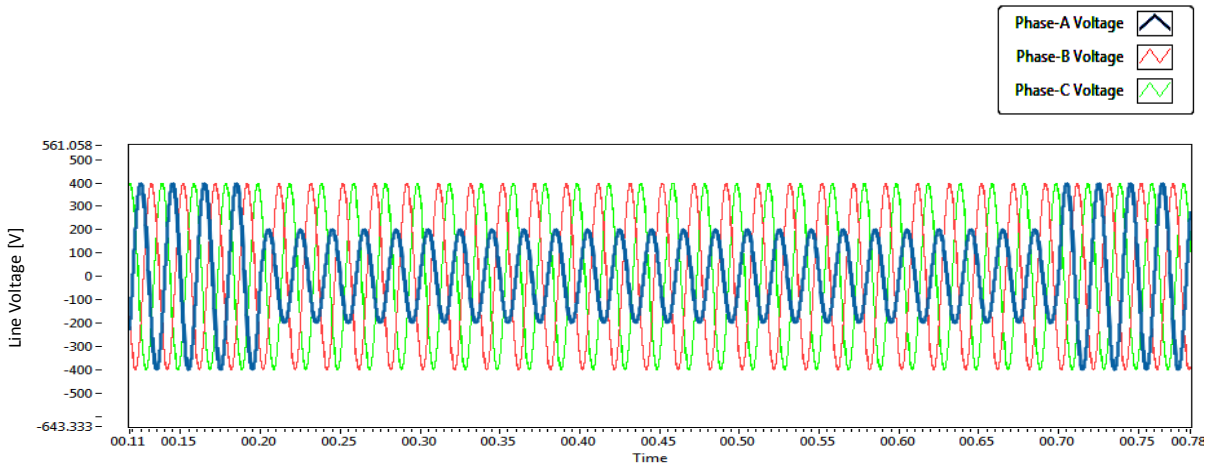
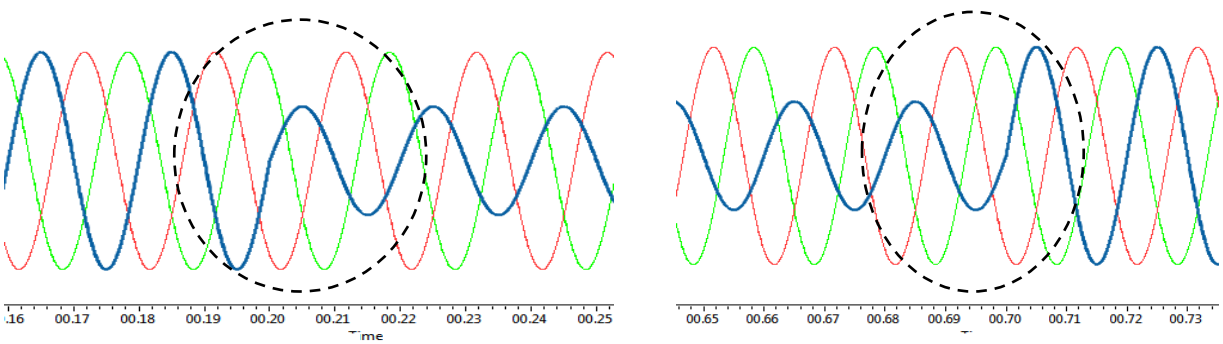


Figure 6.34: Type B Dip Implemented

A 50% voltage dip was implemented on phase-A. Zoomed-in screen shots are shown below in figure 6.35 illustrating the start and end of the dip implemented.



Start time **End time**

Figure 6.35: Zoomed-in Screen Shots of the Dip Implemented

Three phase voltages are then converted into *dq* components. As this is an unsymmetrical dip a negative sequence also appears into the reference frame. Dual vector control was applied to control the negative sequence voltage. Figure 6.36 and 6.37 show the positive and negative sequence *dq* voltages under unbalance condition.

Figure 6.36 reveals positive sequence components. A 50% dip was applied which had a 32% magnitude deviation, calculated from the discussion in figure 6.15. The positive *d*-component went down to almost 330V and the *q*-component stayed at zero.

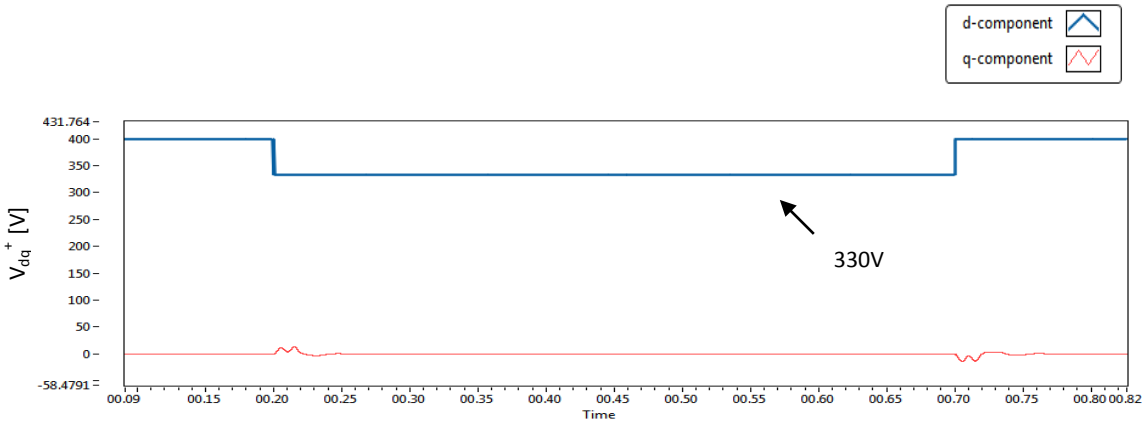


Figure 6.36: Positive *dq* Components of the Type B Dip Implemented

Similarly in figure 6.37 the negative d-component has 7.5% magnitude deviation whereas the *q*-component has a slight AC component with approximately 0% of deviation.

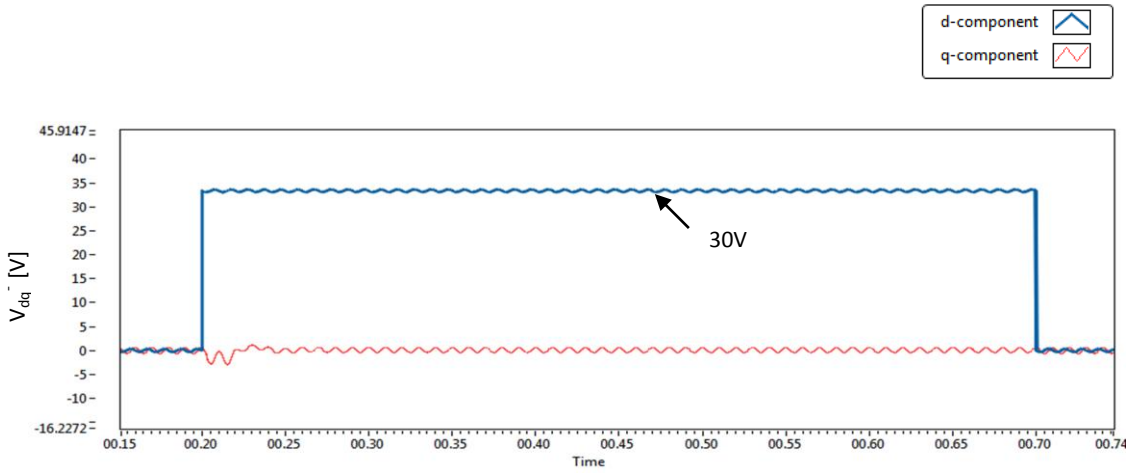


Figure 6.37: Negative *dq* Components of the Type B Dip Implemented

➢ Type E Dip

It reduces the magnitude on two phases while maintaining the third at nominal value. The phase angles are maintained thereby allowing magnitude unbalance to be implemented. Figure 6.38 shows the waveform in which two phases with less magnitude can be seen.

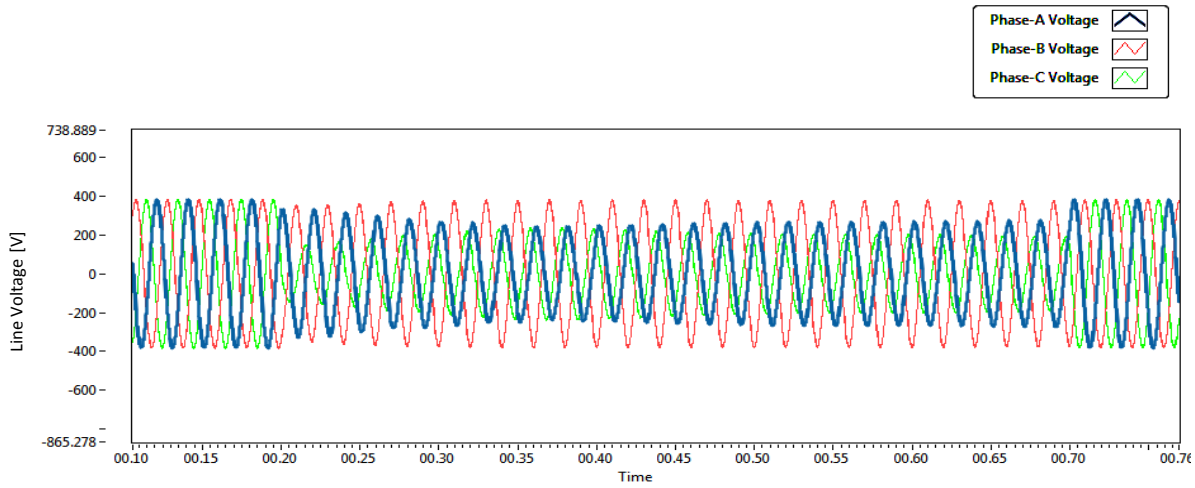
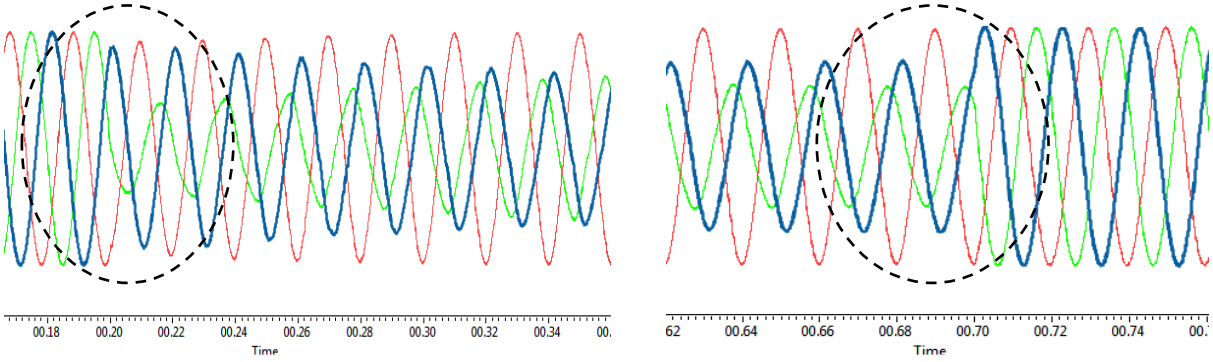


Figure 6.38: Type E Dip Implemented

A 50% voltage dip was implemented on phase-A and C. Zoomed-in screen shots are shown below in figure 6.39 illustrating the start and end of the dip implemented.



Start time **End time**

Figure 6.39: Zoomed-in Screen Shots of the Dip Implemented

Three phase voltages are then converted into *dq* components. Figure 6.40 and 6.41 show the positive and negative sequence *dq* voltages under unbalance condition. Figure 6.40 illustrates positive sequence components. A 50% dip was applied which has a 15% magnitude deviation.

Here the positive *d*-component went down to almost 260V and q-component stayed at zero. It is noticed from the figures 6.36 and 6.40 that positive *d*-component in Type-E dip has less magnitude deviation than Type-B. From the results it is investigated to be 17% less.

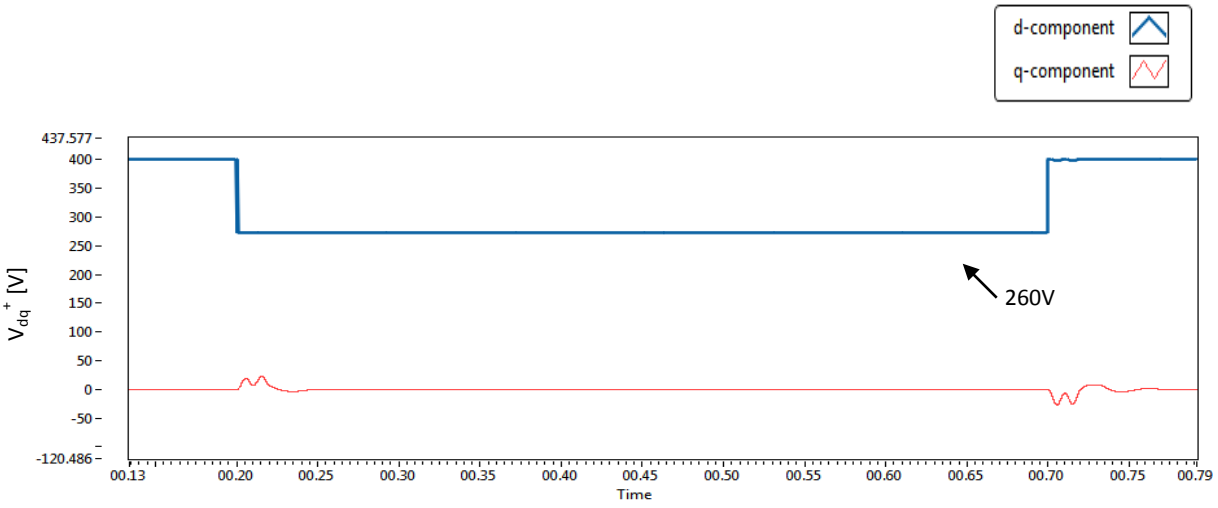


Figure 6.40: Positive *dq* Components of the Type E Dip Implemented

Similarly in figure 6.41 the negative *d*-component has 3.75% magnitude deviation and *q*-component stays at zero respectively. In addition to this a Type-E dip has lower negative *d*-component deviation than Type-B when compared to figure 6.37. It is to be further concluded that the negative *d*-component for Type-E in a three-level converter has less magnitude deviation than that of the two-level converter.

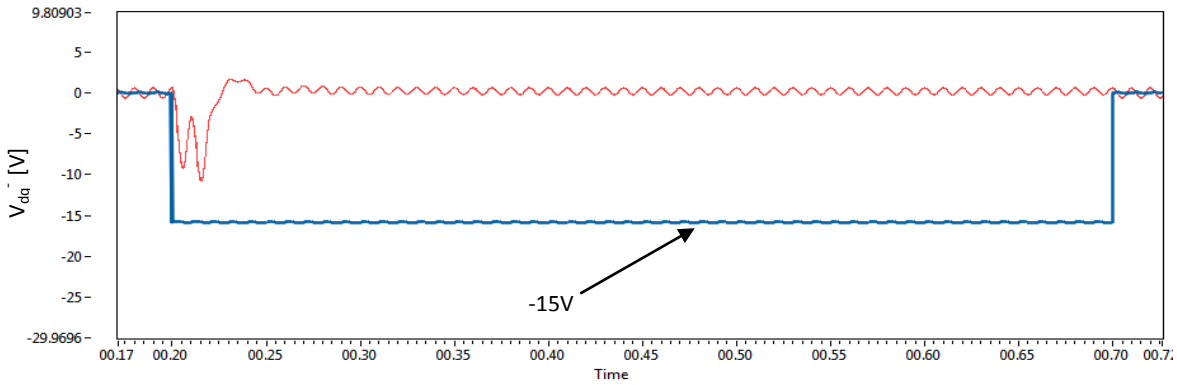


Figure 6.41: Negative *dq* Components of the Type E Dip Implemented

6.2.3.2. Voltage Swell/Overvoltage

In the figure below 50% symmetrical overvoltage is implemented in the system. The output waveform from the three-level converter in inverter mode of operation is shown below.

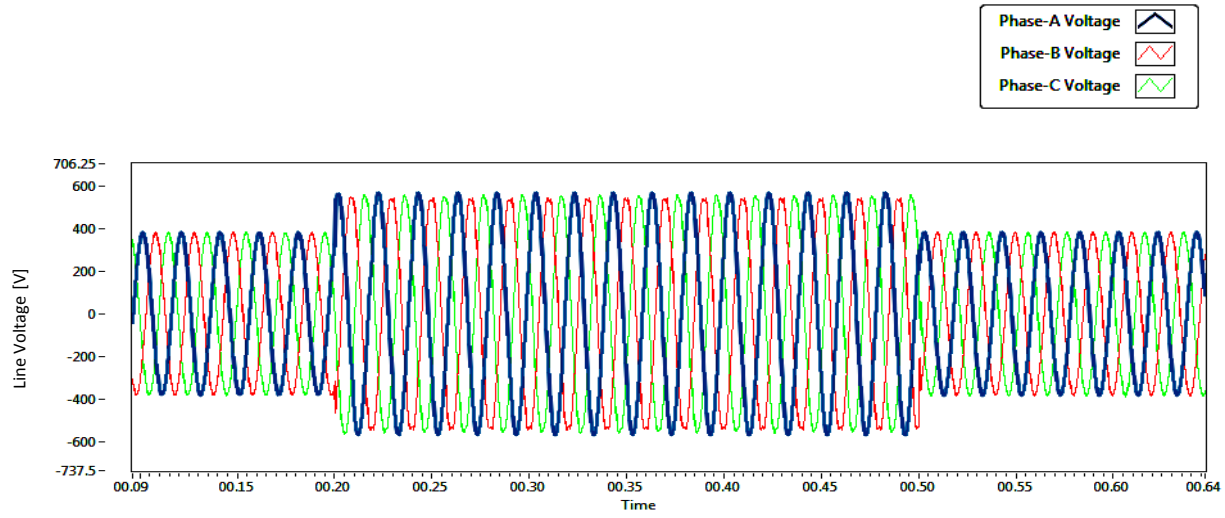


Figure 6.42: Symmetrical Overvoltage Implemented

The overvoltage was implemented on all three phases. Zoomed-in screen shots are shown below in figure 6.43 illustrating the start and end of the overvoltage implemented.

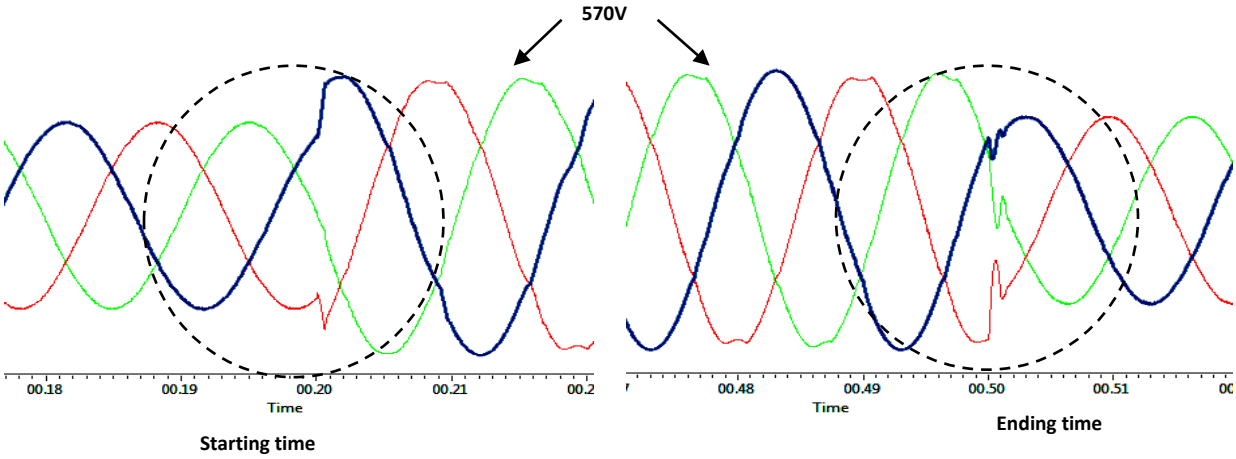


Figure 6.43: Zoomed-in Screen Shots of the Overvoltage Implemented

Now for dynamic response analysis the three phase voltages are converted into *dq* components. As it is a symmetrical overvoltage, in this case there will be no negative sequence component hence positive *dq* waveforms are shown in figure 6.44.

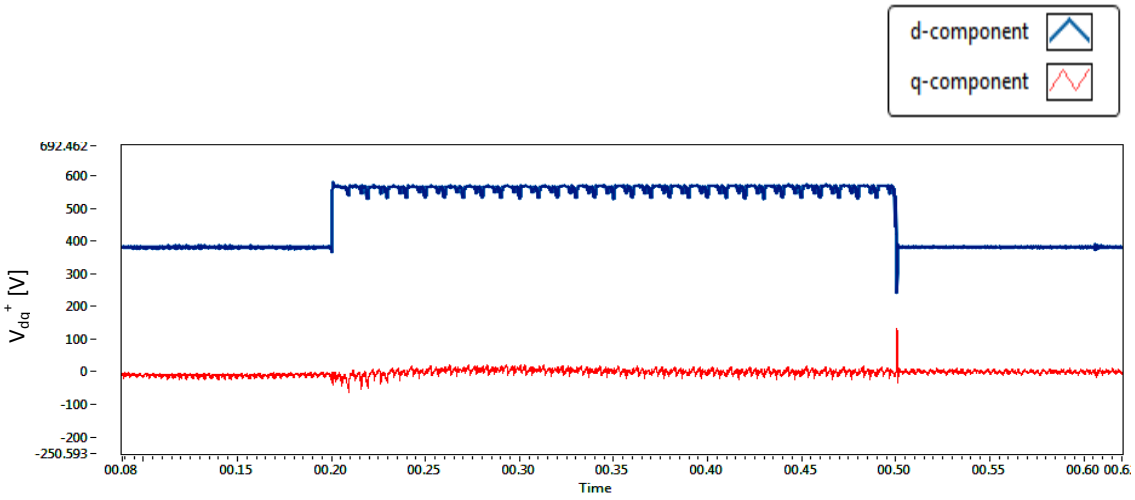


Figure 6.44: Positive *dq* Components of the Symmetrical Overvoltage Implemented

Zoomed-in screen shots of the start and end of the overvoltage are shown below. Figure 6.45 depicts the settling time of the overvoltage and i.e almost 1ms.

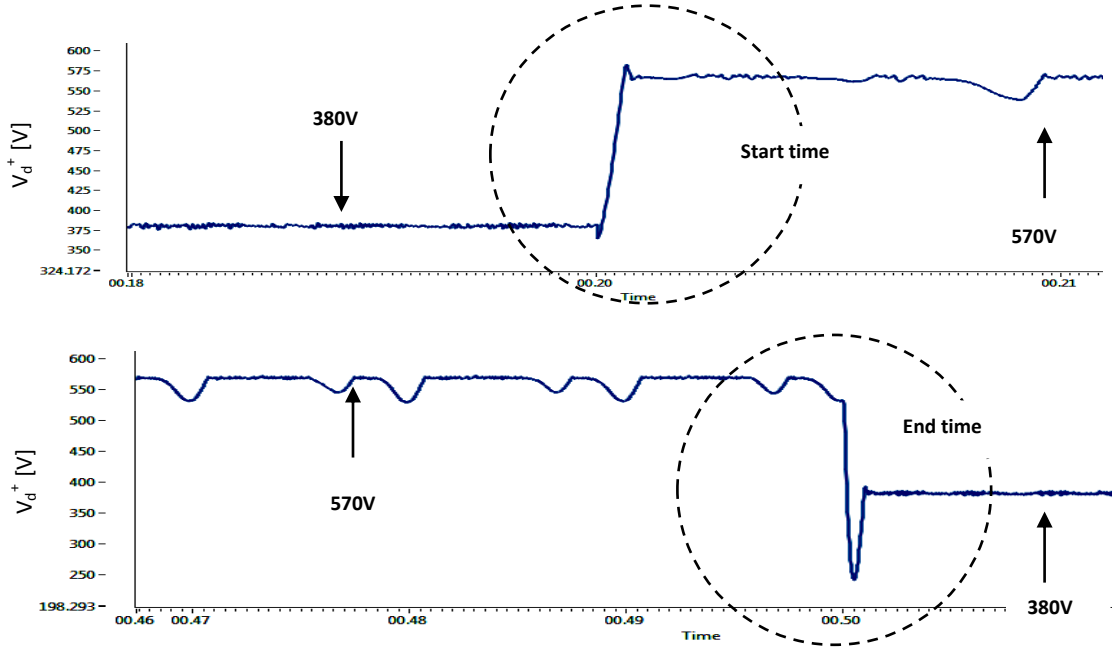


Figure 6.45: Zoomed-in Screen Shots of the *d* Component

6.3. Conclusion

This chapter includes complete simulations of the system. The performance of two main sub-systems of the grid emulator was presented individually. The performance of both converters was analysed on the basis of dynamic response and magnitude deviation calculations. Dynamic response is almost the same for both topologies i.e 1ms. The only advantage with the three-level converter is its low waveform distortion and lower magnitude deviation. The Grid emulator as a whole system was run successfully with steady state voltage regulation. Voltage unbalance conditions were implemented perfectly according to the required set points. It can be concluded that all the system simulations behaved as expected with correct operation of the system.

CHAPTER 7

LABORATORY IMPLEMENTATION

This chapter introduces the experimental implementation of the system in the laboratory. Relevant parameters of the system's components including both the hardware and the software are obtained and discussed. Certain issues which occurred during the implementation are also highlighted.

7.1. Overview of the Laboratory Setup

In figure 1.1 and 3.1 the basic configuration of grid emulator is illustrated. Here the actual setup is shown in the figure below:

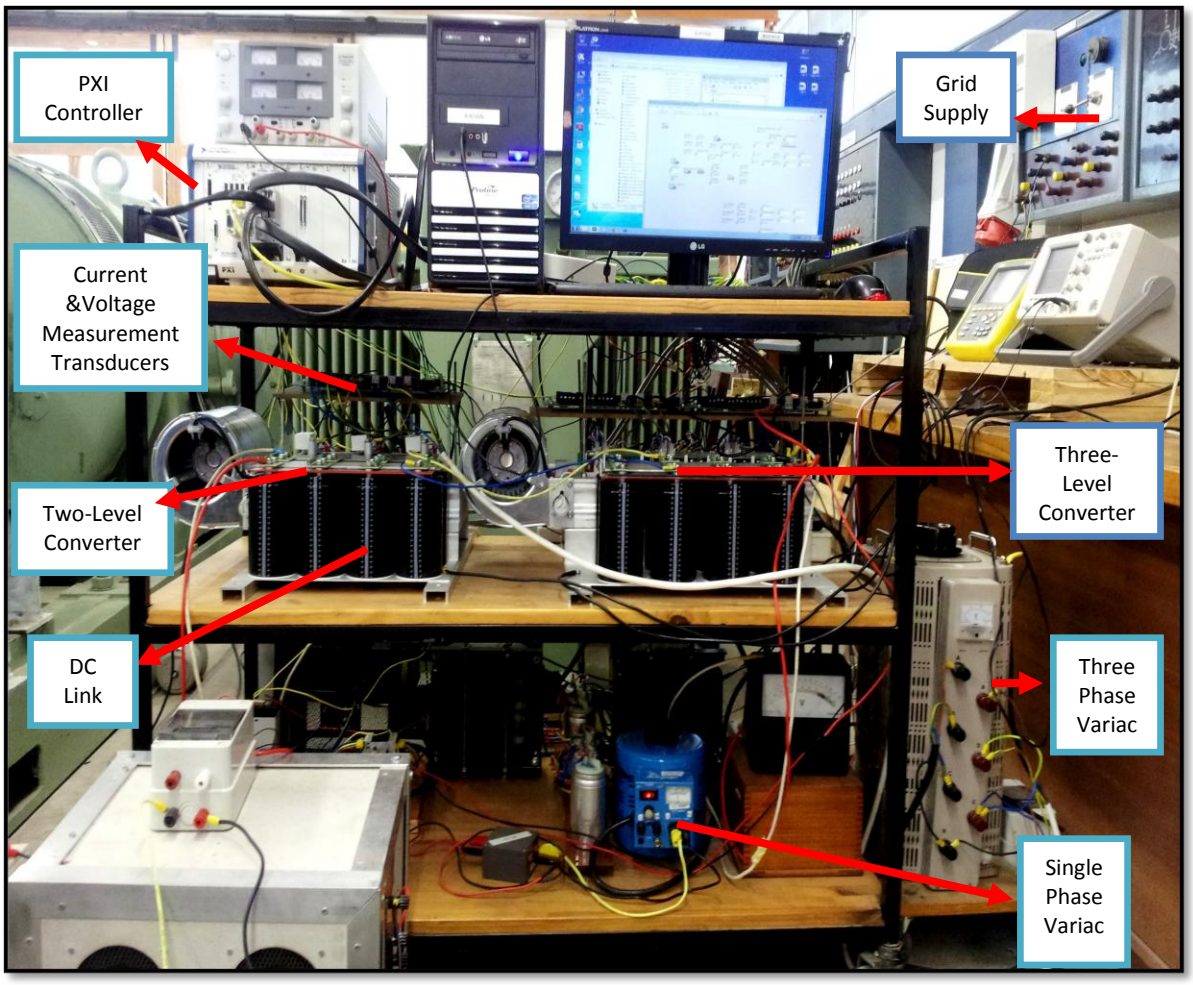


Figure 7.1 : Front View of the Hardware System

In the figure 7.1 the front view of the system is illustrated. Starting from the grid, a three phase variac is connected to it which acts as soft start supply. A voltage line is connected to the voltage measurement transducers to measure the grid voltage and for PLL calculation. Another line is connected to the 'L' filter followed by the current measurement transducer's board. Back-to-back converters can be seen in the middle shelf attached to the DC bus. A single phase variac is also shown, which is used to charge up the DC link. A PXI controller can also be seen on the top. Every block mentioned in this figure is explained in further detail.

In figure 7.2 rear view of the system is shown, illustrating L and LCL filters.

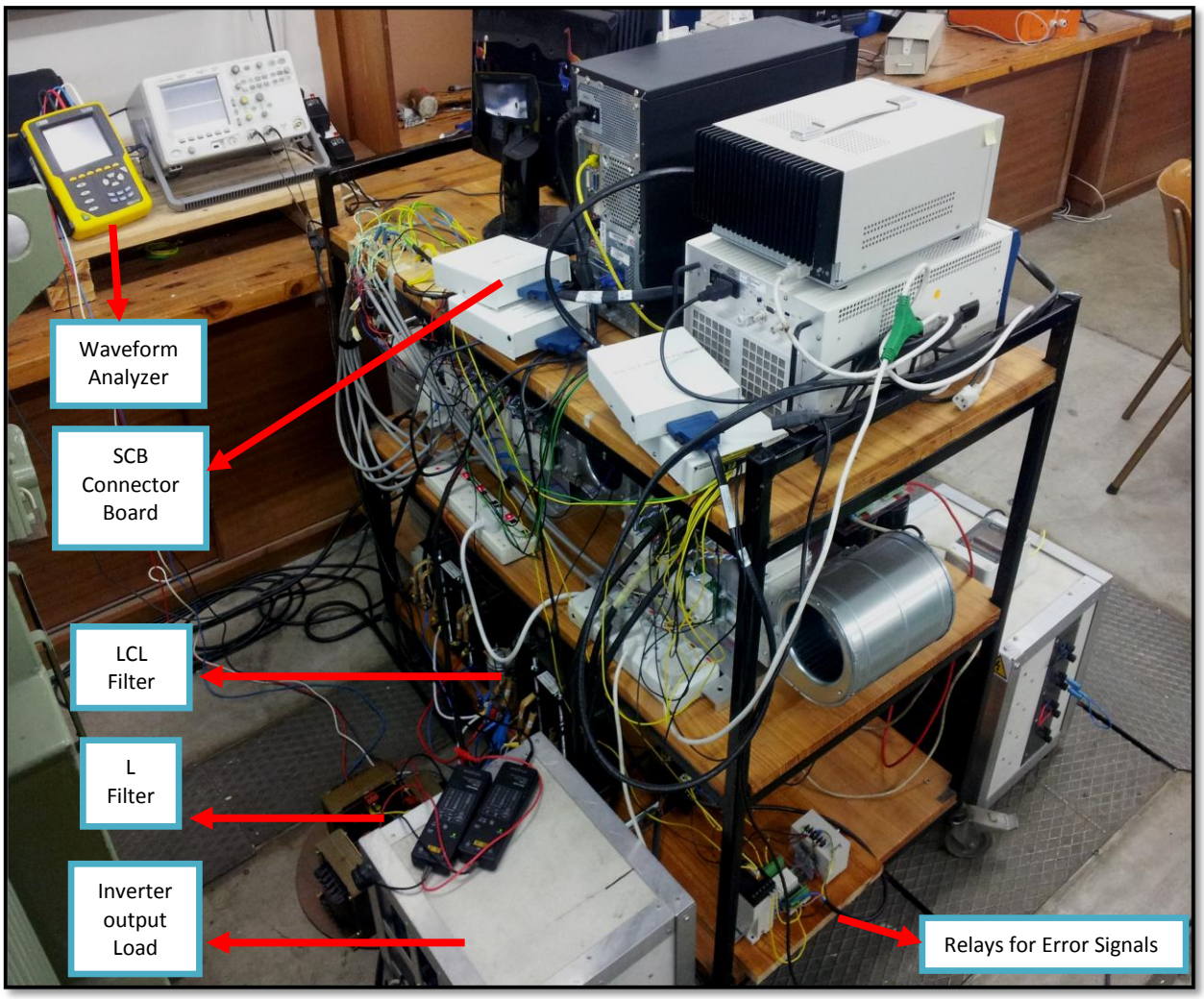


Figure 7.2 : Rear View of the Hardware System

A 1kW load is connected to the LCL filter output which was attached to the inverter. Relays for error signal control can be seen in the bottom. SCB connector boards which are part of the PXI controller, are located behind the computer. Detailed performance of each component is discussed in the subsequent sections.

7.2. PXI Controller

PXI is a PC based controlling medium for measurement and automation systems. It has multi card slot features which add synchronisation with the hardware through the cables. PXI is a high speed economical deployment platform for applications such as consumer electronics, hardware in loop, RF and communication and semiconductors. PXI is rapidly becoming industrial standard with the largest selection of chassis, controllers and timing synchronisation modules.

PXI can be linked up with the PC using Labview software, which is another important product of National Instruments. The measurement and automation explorer provides the interface between the PXI and the Labview [44]

For this thesis two onboard expansion cards were used for processing and measuring as shown in figure below:

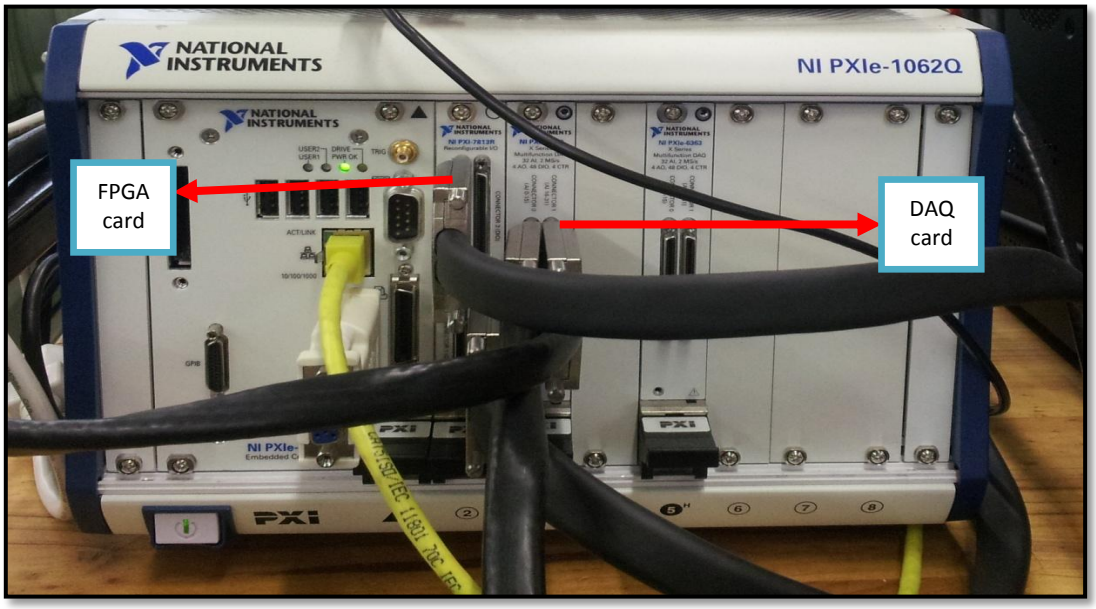


Figure 7.3 : PXI Chassis Mounted with FPGA and DAQ Cards

7.2.1. On-board FPGA card NI-PXI-7813R

7813R has a fast logic rate of 40MHz with 160 configurable digital lines. It has user defined triggering timing and on-board decision making with 25ns resolution [45]. It can be further connected to SCB connector boards with data cables capable of high speed digital pattern generation and are shown in figure 7.4.

It was used for PWM switching and for other triggering components.

Figure 7.4 : SCB Connector Boards for Triggering Attached with Data Cables

7.2.2. Data Acquisition Card DAQ NI PXIe-6363

The e-6363 is an x-series data acquisition card. It has 32 analog inputs with data rate of 2 MS/s single channel and four analog outputs with data rate of 2.88 Ms/s. Moreover it has 48

other digital input output lines timed up to 10MHz [45]. SCB are further used for input output data measurements and are shown in figure below.

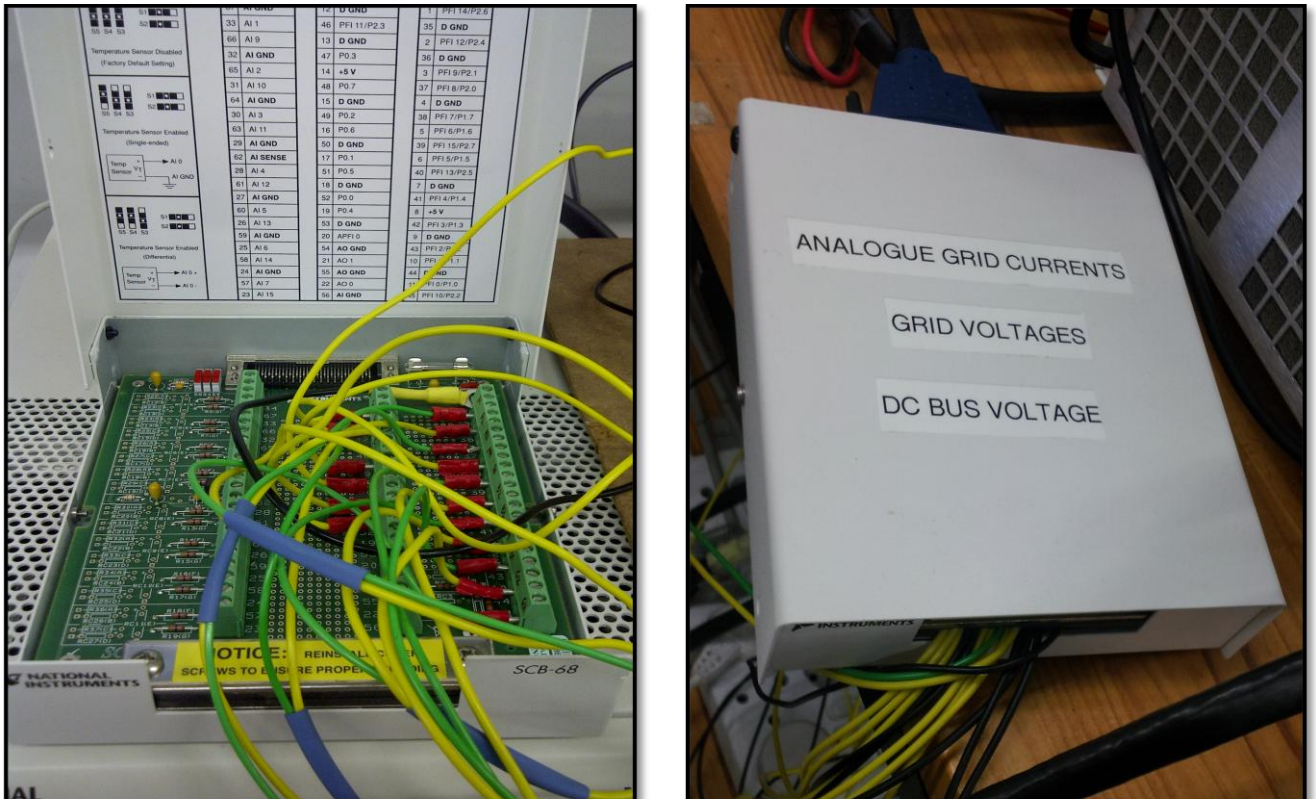


Figure 7.5 : SCB Connector Boards with Lid Open and Closed

7.3. Back-to-Back Converters

For the grid emulation process two back-to-back converters manufactured by Semikron are deployed. It has a built-in DC link with a capacitance of 4900µH. Both converters have a different set of IGBTs with the same type of driver circuit. Pictures of individual and back-to-back converters are shown below in figures 7.6, 7.7 and 7.8.

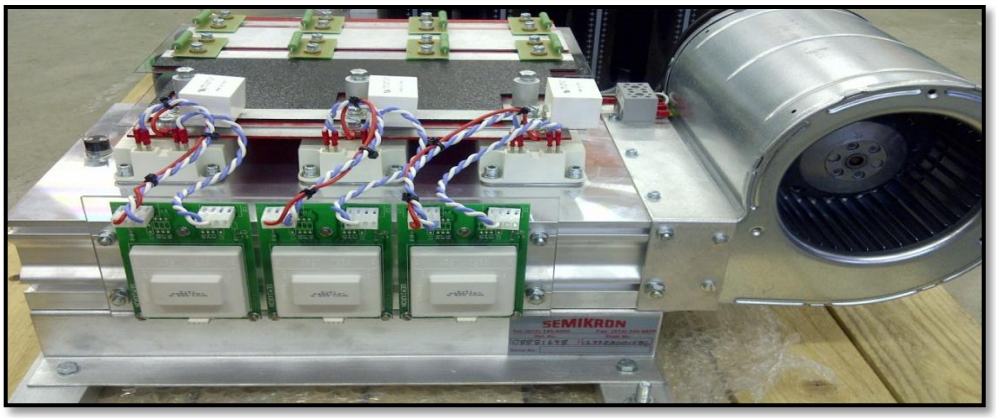


Figure 7.6 : Two-level Converter Unassembled

Figure 7.7 : Three-level Converter Unassembled

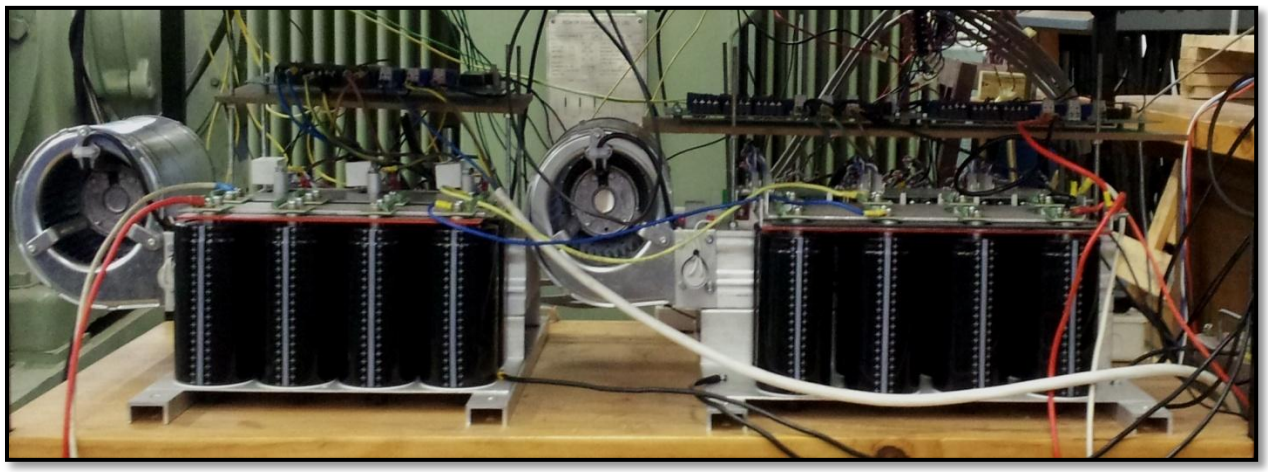


Figure 7.8 : Two-level and Three-level Converters in Back-to-Back Configuration

7.3.1. IGBTS

For a three-level converter a special kind of Semikron 4-Trench IGBT module skim200MLI-12E4 is used for switching purposes. It has four switches per module. The maximum voltage rating is 1200V and the maximum current rating is 200A which enables it to handle maximum ratings of the system. A circuit diagram of skim200MLI-12E4 is given in Appendix C. A hardware picture is shown in the figure below:

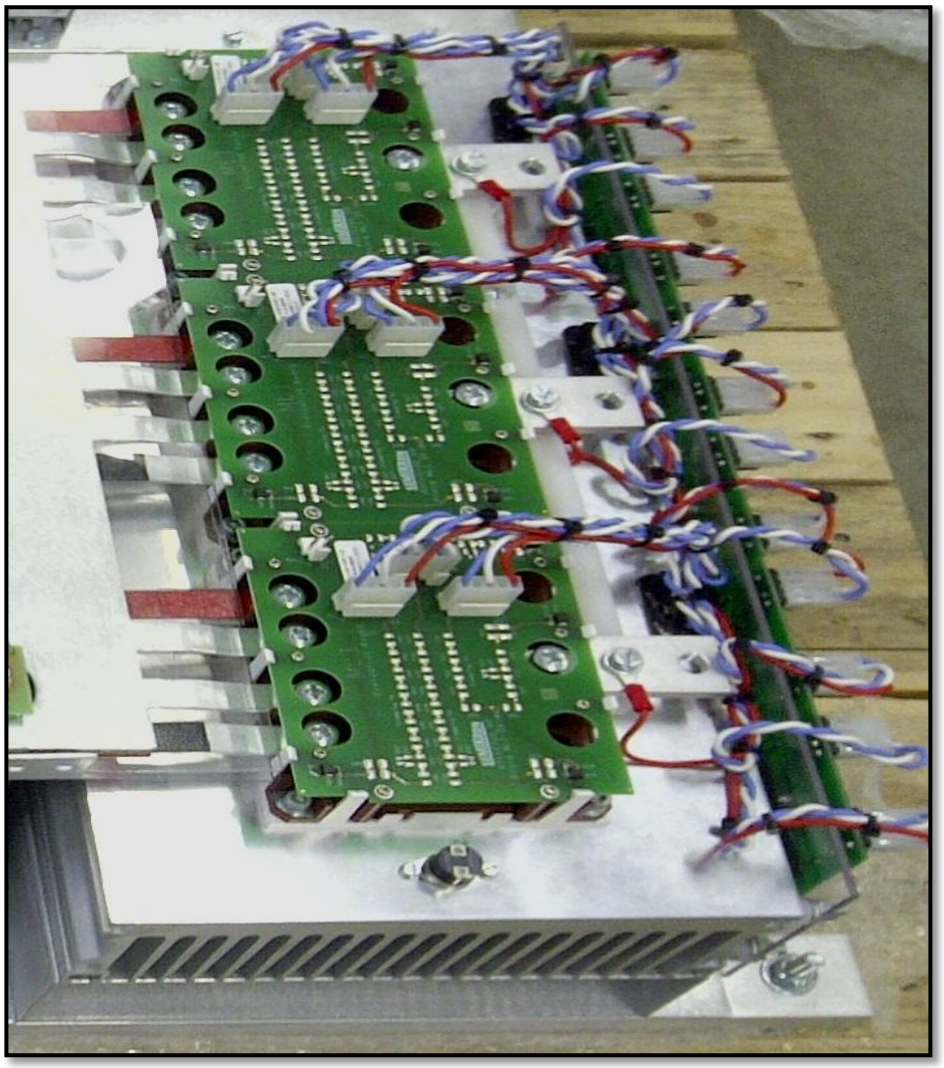


Figure 7.9 : SkimMLI200 IGBT Modules

Semikron SKM145GB123D IGBT modules are used as a switch for the two-level converter. Each module has two switches. It has a maximum voltage rating of 1200V and a maximum current rating of 145A. Picture is shown in the figure below:

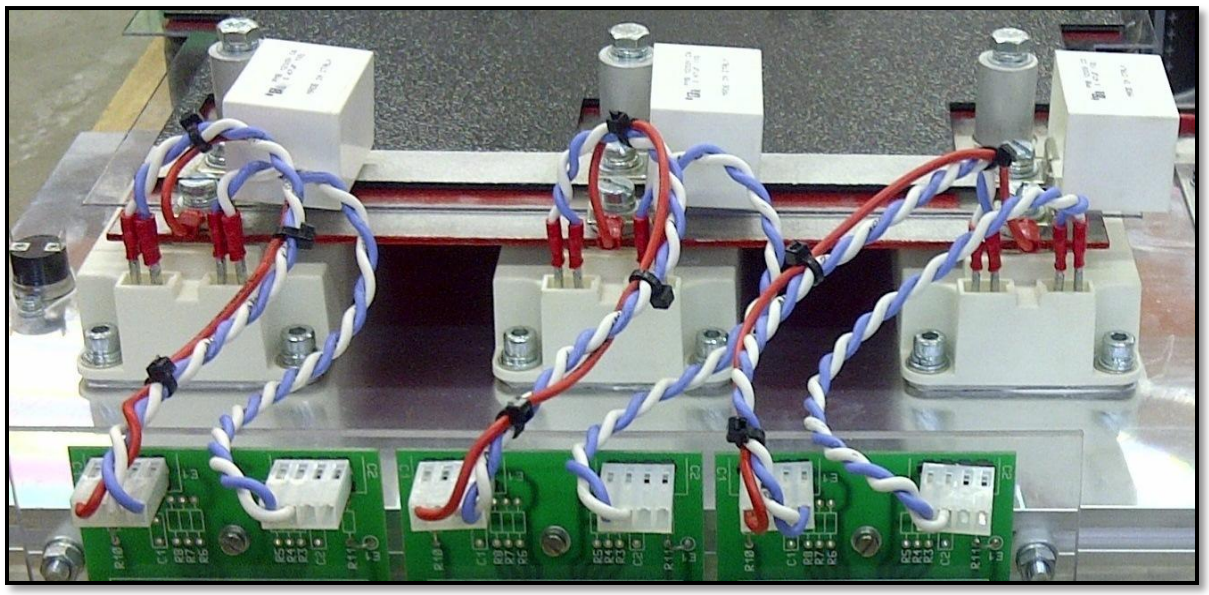


Figure 7.10 : SKM144GB123D IGBT Modules

7.3.2. Drivers

The drivers used for both IGBTs are Semikron SKHI22BR. Each driver has high and low output signals with built in interlock timing to block shorting of the IGBT switches. Collector-emitter voltage V_{CE} across the IGBT is 1200V. If an error is detected by the interlock or collector-emitter voltage monitors, the driver will shut down immediately and produce an error signal.

The V_{CE} monitoring reference is set by choosing a suitable resistor R_{CE} and the delay before the monitoring is activated and set with parallel capacitance C_{CE}. All components' values can be estimated from the data sheet given in figure 7.11[46].

The error signal is 15V under normal conditions and it switches to 0V in case of error value.

Component	Function	Recommended Value
R_{CE}	Reference voltage for V_{CE}-monitoring $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}4$ (1) with R_{VCE} = 1kΩ (1700V IGBT): $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}8$ (1.1)	10kΩ < R_{CE} < 100kΩ 18kΩ for SKM XX 123 (1200V) 36kΩ for SKM XX 173 (1700V)
C_{CE}	Inhibit time for V_{CE} - monitoring $t_{min} = \tau_{CE} \cdot \ln\left[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)}\right]$ (2) $\tau_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$ (3)	C_{CE} < 2,7nF 0,33nF for SKM XX 123 (1200V) 0,47nF for SKM XX 173 (1700V) 0,5µs < t_{min} < 10µs
R_{VCE}	Collector series resistance for 1700V IGBT-operation	1kΩ / 0,4W
R_{ERROR}	Pull-up resistance at error output $\frac{U_{Pull-Up}}{R_{ERROR}} < 15mA$	1kΩ < R_{ERROR} < 10kΩ
R_{GON}	Turn-on speed of the IGBT [4]	R_{GON} > 3Ω
R_{GOFF}	Turn-off speed of the IGBT [5]	R_{GOFF} > 3Ω

Figure 7.11 : Components Value Calculation[46]

The circuit diagram of the driver can be found in Appendix C. Figure 7.12 shows a driver board mounted on the converter stack.

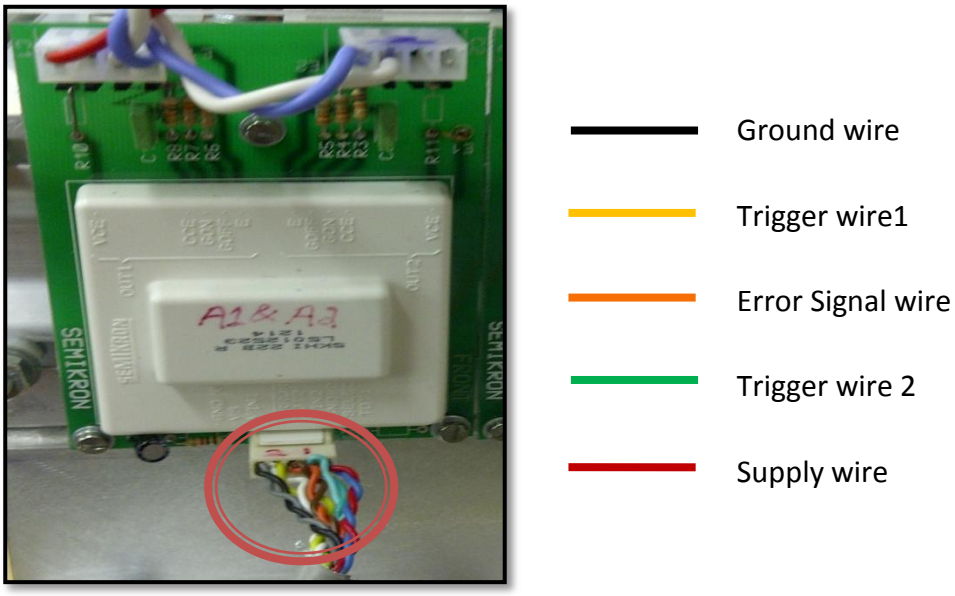


Figure 7.12 : Driver Board with Signal Wires Configuration

7.3.3. Voltage Shifter board

FPGA signal output from the SCB (shielded connector board) is 3.3V. However the SKHI22B driver board triggers at 5V. In order to match the required voltage a circuit was designed, which performs an 'and gate' function on arrival of a signal and gives a regulated 5V at the output. The voltage shifter board is shown in the figure below:

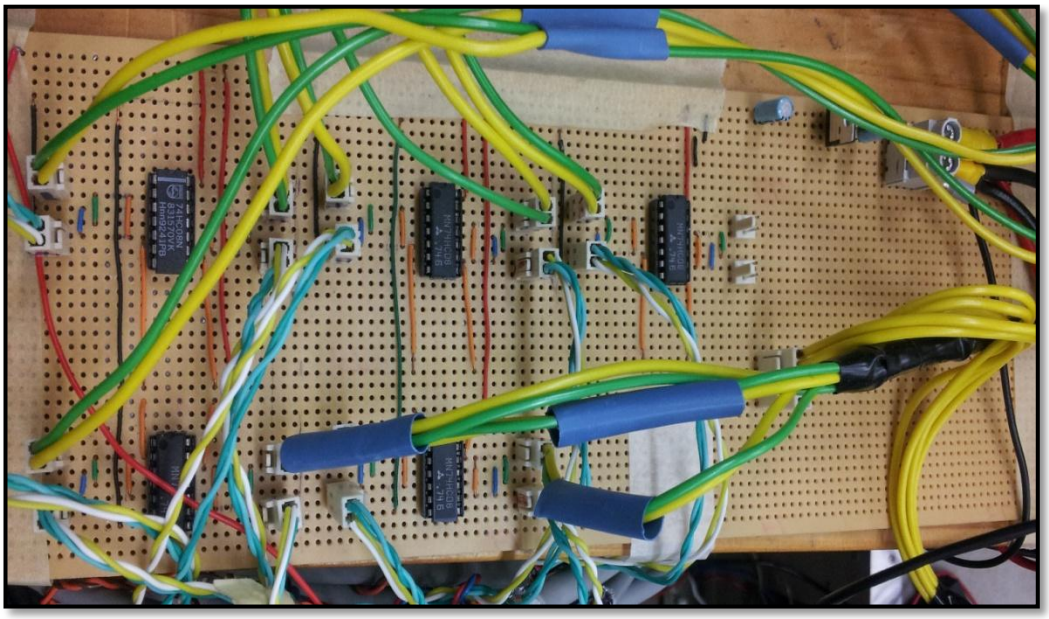


Figure 7.13 : Voltage Shifter Board

7.4. Instrumentation and Measurement

In this section all the measurements are implemented. The operation of current and voltage transducers is discussed with the calculations of all the mounted components on the PCBs. Moreover, this section also discusses its interface with the analog signals and the controller.

7.4.1. Current and Voltage Measurement

LEM Modules are used to measure the current and voltages of the entire system. Three current sensors are used for the grid current measurement. Seven voltage sensors are used, three for the grid side to check PLL, three for the load side output and one for the DC link voltage. The

sensors are mounted on custom PCBs which are further mounted on the converter. The circuit diagrams for the boards can be found in Appendix C.

➢ Current Measurement LEM Modules

LA100 current LEM modules were used. Primary nominal rms current is 100A, whereas on the secondary side it is 50mA. Thus it gives an attenuation ratio of 2000:1 between the primary and secondary side currents. If R_{out} is calculated to be 200Ω then from the ohm's law output voltage for 100A will result in 10V. The operation of current measurement module is shown in figure 7.14.

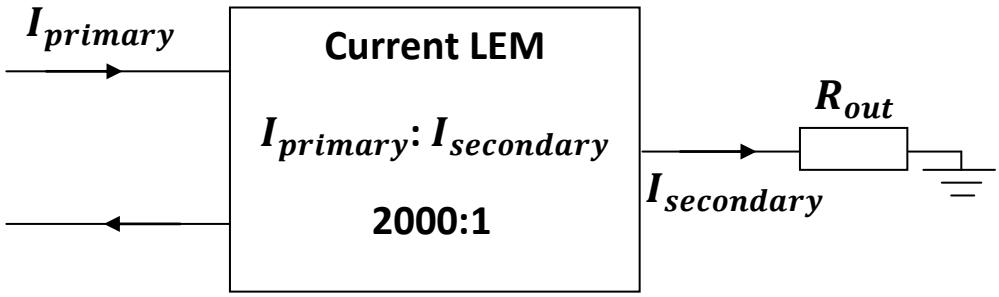


Figure7.14: Operation of Current Measurement LEM

A picture is shown in figure 7.15 where current measurement LEM modules are mounted on the converter stack.

Figure 7.15: Current Measurement LEM Modules PCB

➢ Voltage Measurement LEM Modules

LV25 voltage LEM modules are used. Primary nominal rms current is 10mA, whereas on the secondary side it is 25mA, thus giving it an attenuation ratio of 1:2.5 between the primary and secondary side currents. Its primary current measuring range is 10mA which with primary resistance of 100kΩ gives 1000V. If R_{out} on the secondary is calculated to be 200Ω then from the ohm's law output voltage for 25mA will result in 5V. That means the voltage ratio between primary and secondary would be 1000:5. Operation of voltage measurement module is shown in figure 7.16.

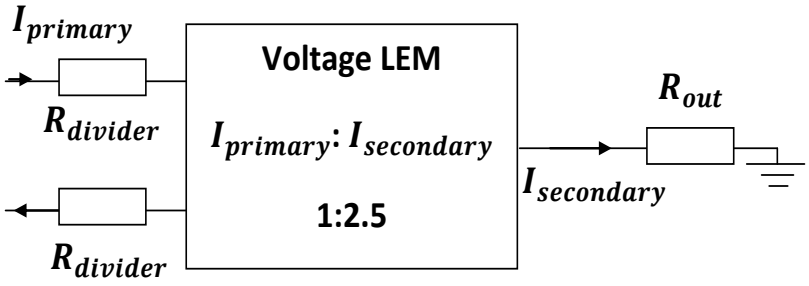


Figure7.16: Operation of Voltage Measurement LEM

A picture is shown in figure 7.17 where voltage measurement LEM modules are mounted on the converter stack

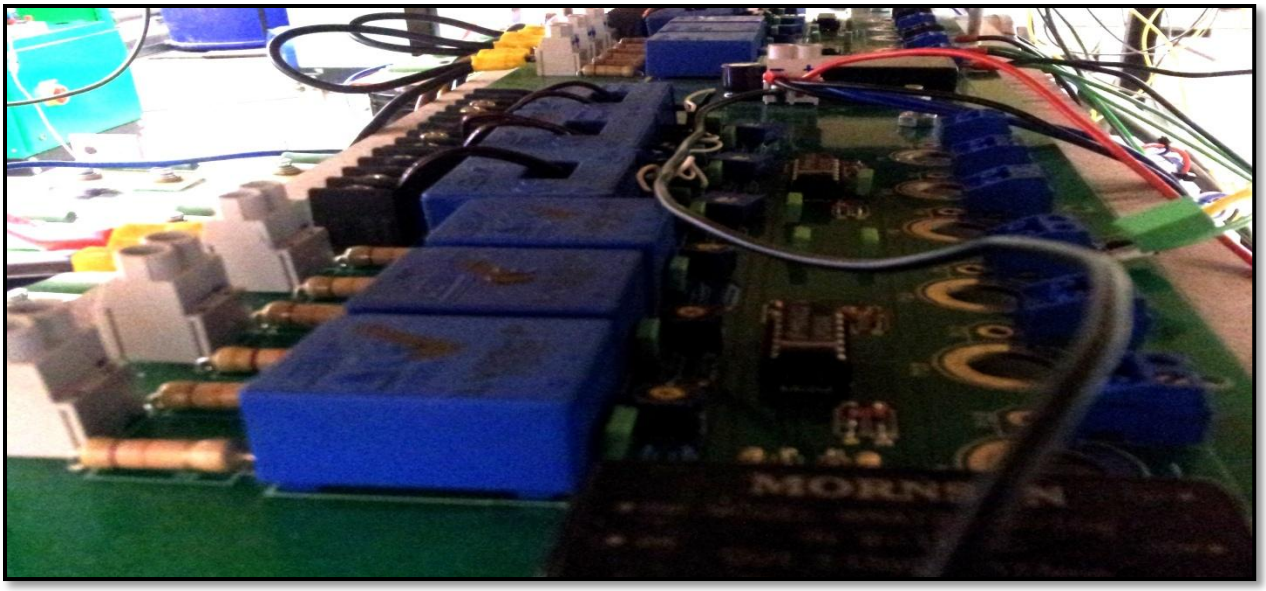


Figure 7.17: Current Measurement LEM Modules PCB

7.4.2. Error Signals and Relays

All error and triggering signals related to emergency switching flows to a box which has voltage divider and operational amplifier buffer circuitry in it. The circuit diagram can be found in Appendix C. Signals sent through a voltage divider regulates the voltages to 0-5V level. The resulting signals are then passed through a unity gain operational amplifier buffer circuit with clamping diodes. This prevents large voltages being sent to the digital inputs and outputs in the case of a circuit malfunction. Both contactors are then controlled by the switching relays being triggered through the operational amplifier circuit. Error signal wires are further connected to converter driver boards. Figure 7.18 shows the whole protection circuit mounted on the board.

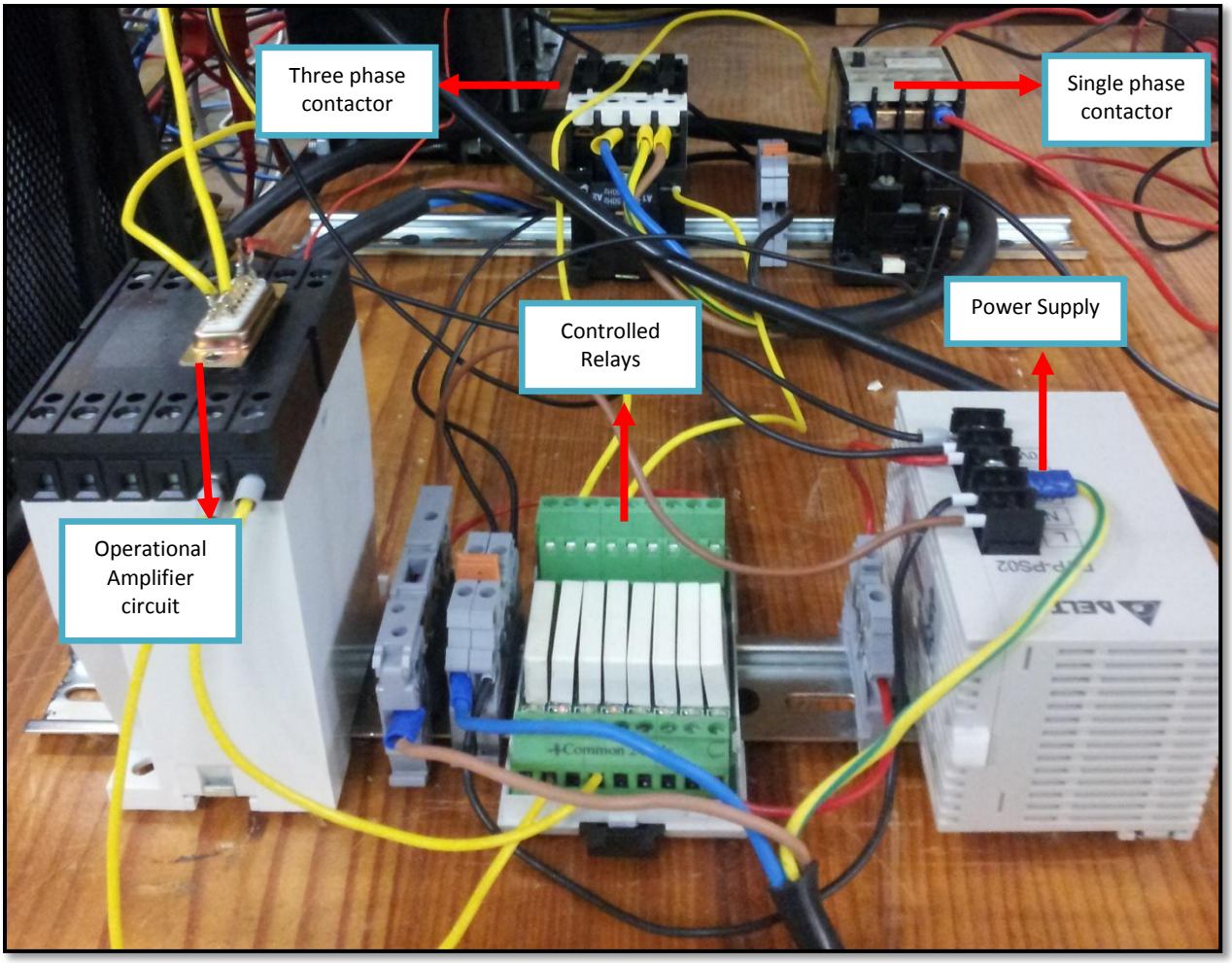


Figure7.18: Error and Relay Control Circuits

A three phase contactor shown in the figure 7.18, provides a connection between a grid and a grid side converter, whereas the single phase contactor charges the DC link when decoupled from the load side converter. If the converter or DC link voltage rises beyond the limit, error signal shuts down the contactors, which ceases the power flow into the system.

7.5. Filtering

Two filters are used on both sides of the system. On the grid side a simple L filter for filtering grid current and in the same manner an LCL filter was employed onto the load side for improved load voltage. Specifications and design of the filters is already discussed in detail. Figure 7.19 shows the filters setup

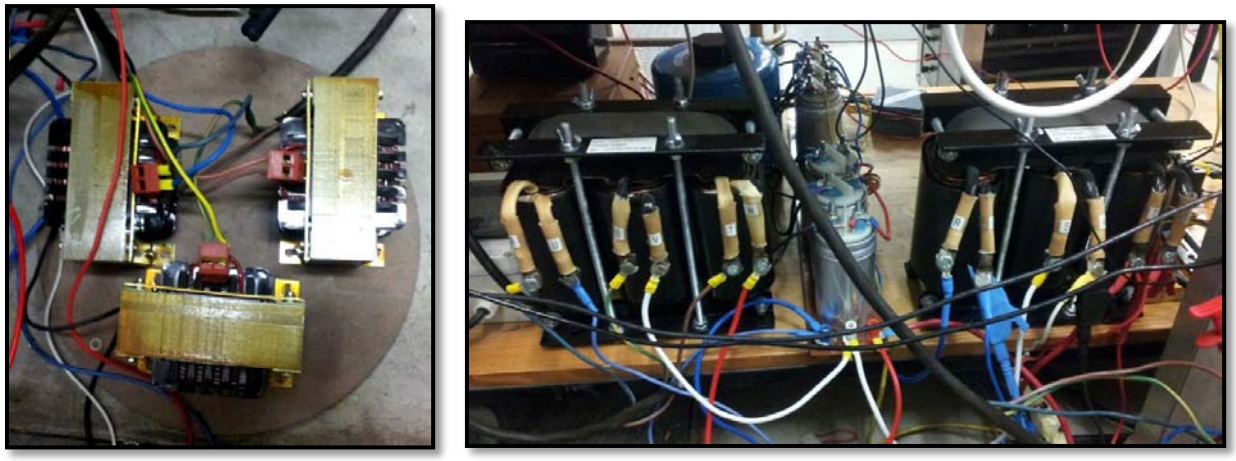


Figure7.19: L and LCL Filter Setup

7.6. Conclusion

This chapter presented the laboratory setup of the grid emulator. Equipment that was used to deploy the system was discussed in detail. A PXI software controller was introduced. Back-to-back converters with their components selection and calculations were estimated. Implementation of measurement transducers was examined. Protection of the error signals with the help of contactors was also explained in depth.

CHAPTER 8

EXPERIMENTAL RESULTS and DISCUSSION

In this chapter experimental results are presented and compared to simulation results presented in chapter 6. The results were obtained from the experimental setup discussed in chapter 7. Comparison of the two converters is made on the basis of the dynamic response and magnitude deviation calculations, which is explained in subsequent sections. The relevant comparisons to analytical and simulated results are also discussed. Finally the correct operation of the grid emulator is confirmed.

The main theme of this thesis is to develop a grid emulator for generating different voltage unbalances. A back-to-back converter topology was used to achieve a controlled flow of bi-directional power, as discussed in earlier chapters. An in-depth analysis of a two-level and a three-level converter connected in a back-to-back configuration was also discussed. The system topology is presented in figure 8.1. Detailed comparisons are done with the aid of experimental results obtained from the hardware implementation.

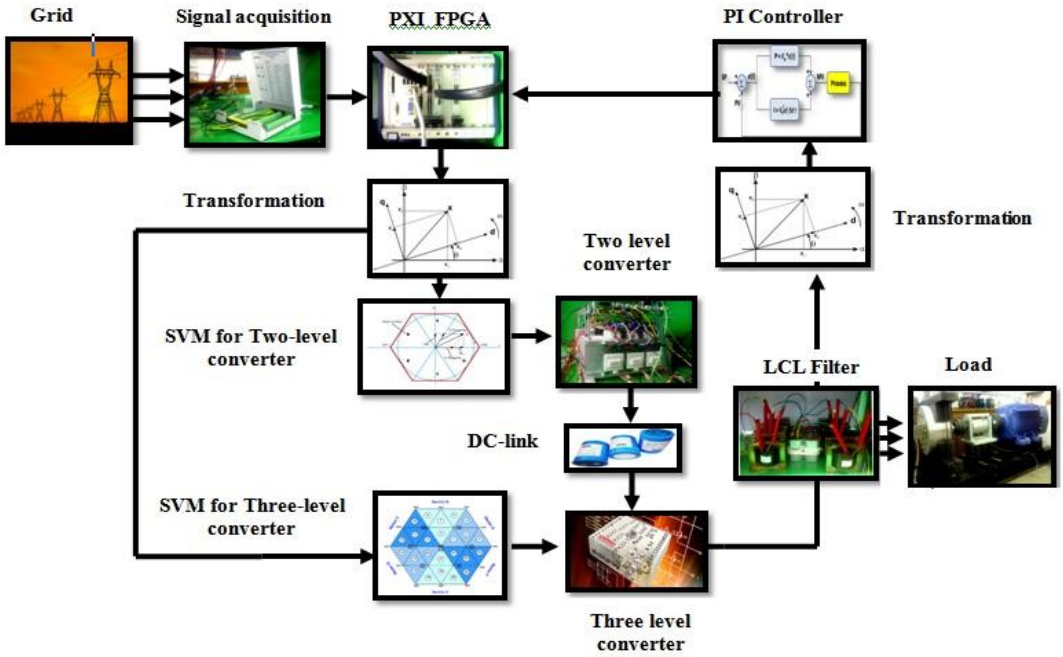


Figure 8.1: Block Diagram of the Grid Emulator implemented experimentally

With reference to figure 8.1 the structure of the system is explained. It can be seen that one converter is connected to the grid. The other converter has a 1kW load attached to its output through an LCL filter. The switching frequency was set to 10kHz and the DC link nominal voltage was set to 800V for all the operations. Voltages of each phase were measured from the midpoint of the filter capacitors. Voltage oriented control was implemented with the current loop controller gains designed in chapter 5. For unbalanced conditions dual vector control was implemented. Positive and negative sequence components were extracted and manipulated to achieve stable control. In this chapter all the results are made for the line-to-neutral rms converter voltages. Furthermore, all the waveforms presented in this chapter are from the real time controller output and the default time scale is given in ticks/sec (National Instruments PXI term). Since the processor speed was 40MHz and the switching frequency was set to 10 kHz, it gives 4000 ticks per second. Thereby converting the time scale into seconds by applying the following formula, $\frac{Point\ B - Point\ A}{4000}$. The resulting time axis in seconds is superimposed on each figure in the subsequent sections.

8.1. Test Setup

There are two sides of the emulator, grid side and the load side. The grid side converter controls the DC link voltage and the load side converter performs as an inverter. There are two tests performed with the system. In the first test, a three-level converter is on the grid side whilst a two-level converter is on the load side. In the second test, a two-level converter is on the grid side whilst a three-level converter is on the load side.

Full system was tested with both converters being connected in back-to-back configuration. For easy comparison between the two converter topologies the test results are shown in two complete sections named with the converter topology.

8.2. Two-level Converter

The two-level converter was first tested as a grid-side converter (active rectification mode of operation) connected to the three-level converter on the load side. Then it is tested as a load-

side converter (inverter mode of operation) connected to the three-level converter on the grid side as discussed in section 6.1.

8.2.1. PWM Switching Signals of the Two-Level Converter

The SVPWM technique was used to control the converters as discussed in chapter 3. The PWM switching signals developed in the Labview environment, which were applied to the converter through the FPGA hardware mentioned in chapter 7. The output waveforms were then analysed in a Labview scope window and on oscilloscope.

An oscilloscope plot of the line-to-neutral PWM waveform for phase-A is shown in figure 8.2. The filtered PWM waveform for phase-B which shows the fundamental line-to-neutral voltage waveform is also shown in figure 8.2:

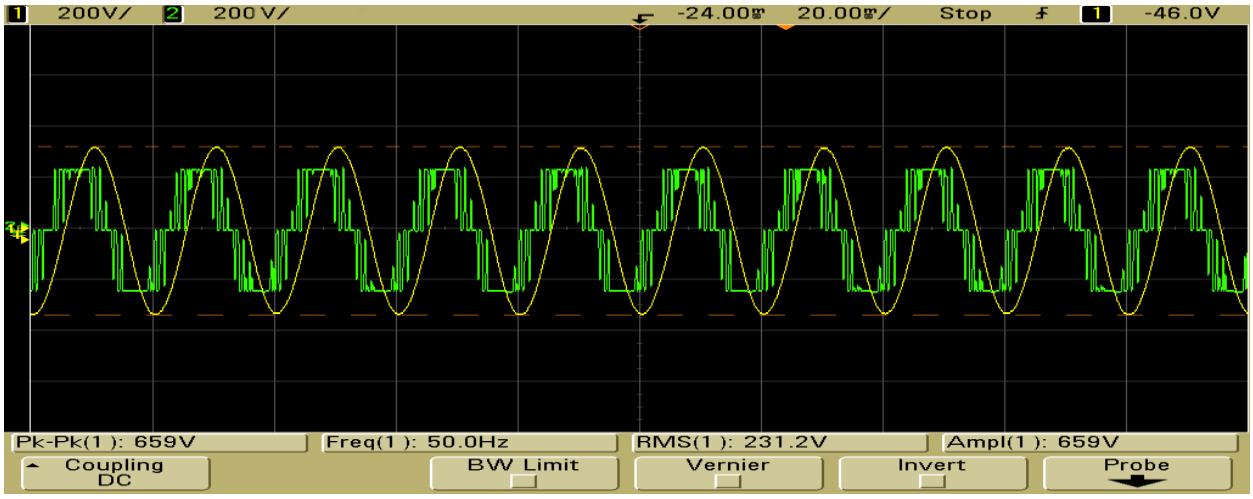


Figure 8.2: Van Line-to-Neutral Before Filtering and Van Output Voltage

8.2.2. Active Rectification Mode of Operation

The tests performed on the two-level converter were implemented to control the DC link voltage. This operating mode is also called active rectification. Step responses were performed in order to confirm the correct operation of the system.

The dynamic response of the two-level converter in rectifier mode was analyzed. A step change in the DC link voltage results in a proportional change to the grid current. The

simultaneous change in voltage and current was done to verify the closed loop stability of the control system. Figure 8.3 below presents the dynamic response of the converter. Change in the DC link voltage set point was stepped down from 300V to 230V and then stepped up from 190V to 310V. Figure 8.3 shows a settling time of 0.80s and 1.0s respectively. The response time determined in chapter 5 from the controller design was much faster as compared to this actual response. Increasing the controller gains can further speed up the step response of the DC bus, but it introduces oscillations in the waveform which could badly affect the stability of the system.

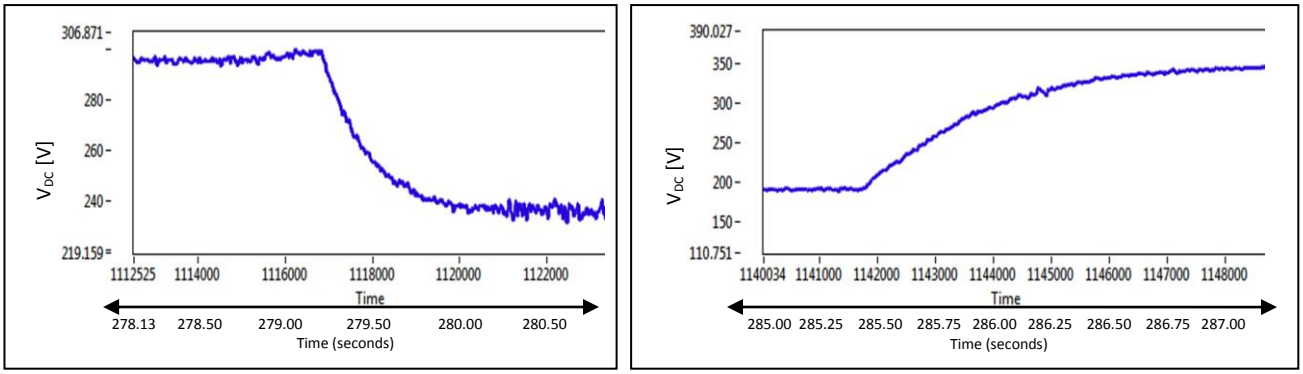


Figure 8.3: Step Response of the DC Link Voltage

The effect of the step down in the DC-link voltage on input grid currents is shown in the zoomed-in figure 8.4. The inductors on the input of the converter reduce the switching ripple and ensure sinusoidal grid currents. The step creates a change in the grid currents at the same instance when the DC link voltage step was applied. When a DC link voltage step was applied, a non-zero value of reactive power appeared. However, this reactive component only appears for a few μs during the transient. With constant impedance load across the DC link, the increase in V_{DC} should correspond to a slight boost in current on the grid side.

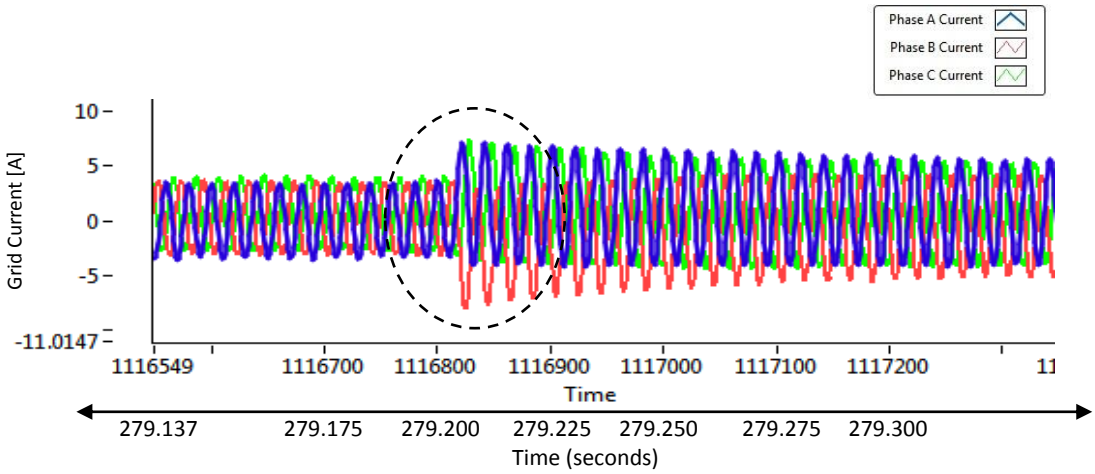


Figure 8.4: Grid Current Response to a Step DC Link Voltage

Steady state grid current waveforms after the first step change in the DC link voltage are shown in the zoomed-in figure 8.5.

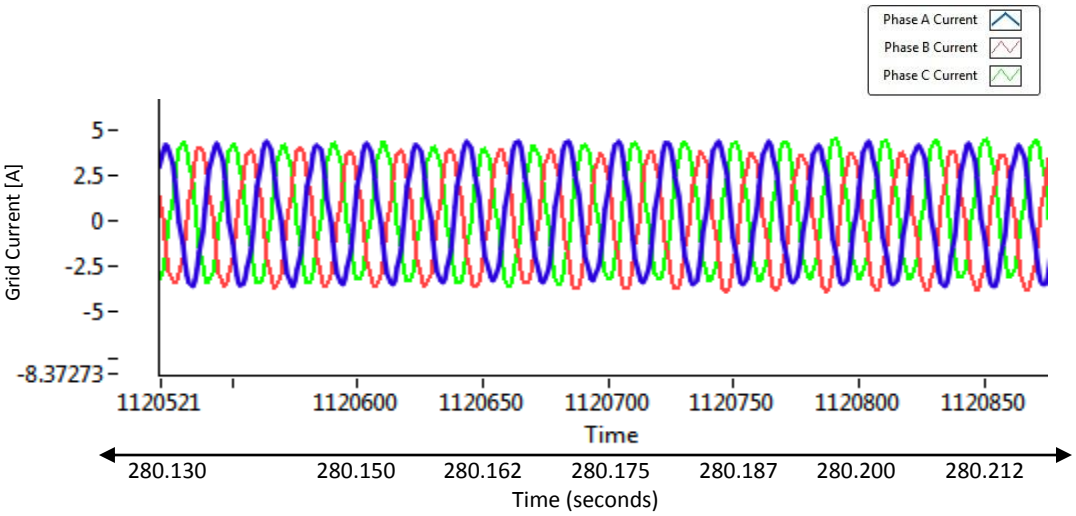


Figure 8.5: Steady State Grid Currents After Step in DC link Voltage

The three-phase current response was recorded when the second step from 200V- 320V was applied and is presented in the figure 8.6:

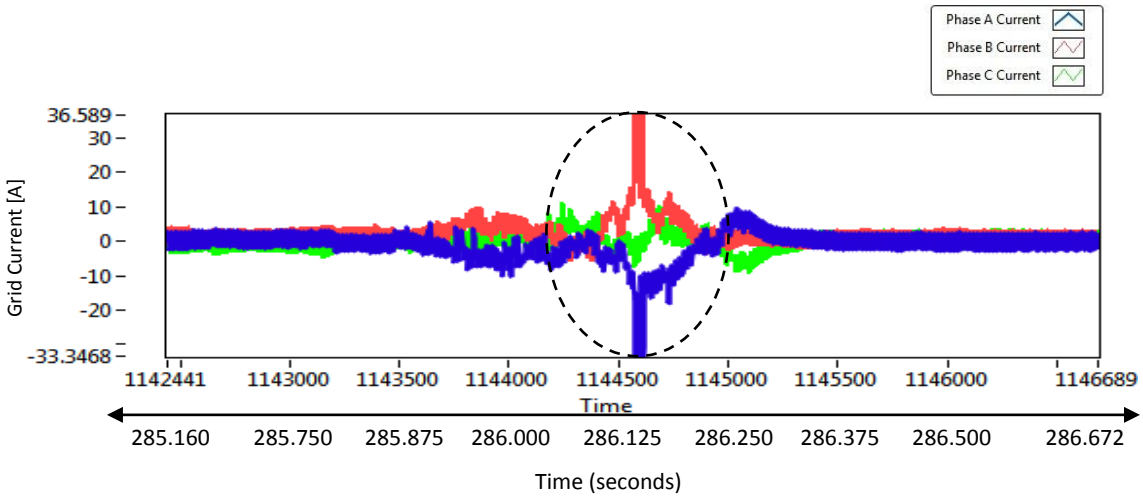


Figure 8.6: Grid Current Affected by DC Link Voltage Step

A high ripple current can be seen which results from the transient created by the DC voltage step on the grid side.

8.2.3. Inverter Mode of Operation

The two-level converter is operated here in inverter mode connected to the DC link controlled by the three-level converter. This will be further analysed in subsequent sections. As mentioned earlier, the main objective of this thesis is to produce different voltage variations on the output of the grid emulator connected to a load. The voltage unbalances implemented experimentally in this thesis are under-voltage (dip) and over-voltage (swell).

8.2.3.1. Voltage Dips/Sags

In this thesis, only the magnitude unbalance of dip types are implemented. In particular type A, B and E dips will be considered. Dual vector control was implemented to control the output of the converter in order to implement the dip on each phase and hence to achieve the intended unbalance. Different loads were then used to evaluate the steady voltage regulation. For all experimental results calculations a 1kW passive load was rated standard.

- **Type A Dip**

The type A dip was introduced by changing the Va, Vb and Vc reference values as shown in control figure 5.14. This reduces the magnitude on all three phases. The phase angles are

maintained at 120° thereby allowing a symmetrical change in magnitude to be implemented as shown in figure 8.7.

Experimental results of the simulations conducted in section 6.1.3 are presented here. Figure 8.7 shows the experimental output voltage of the emulator with a two-level converter in inverter mode of operation. The change in magnitude on all three phases can be seen.

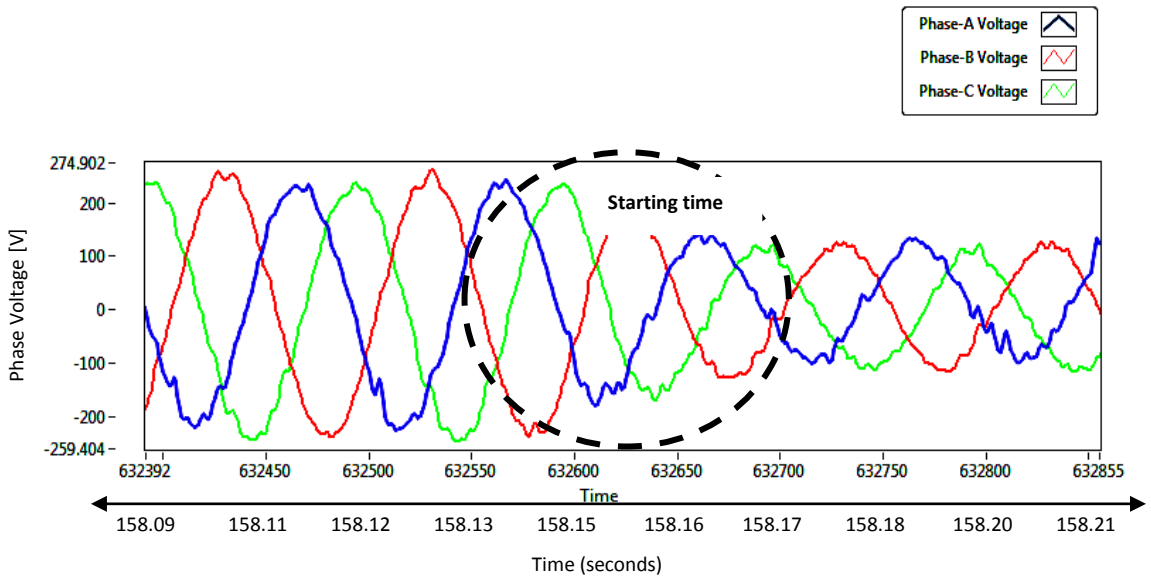


Figure 8.7: Start of the Type A Dip Implemented

A 50% voltage dip was implemented. The start and end time of the dip are shown in the figures 8.7 and 8.8 respectively. Figures show the correlation with the waveforms in figures 6.9. It shows approximately the same spectrum quality as in simulation.

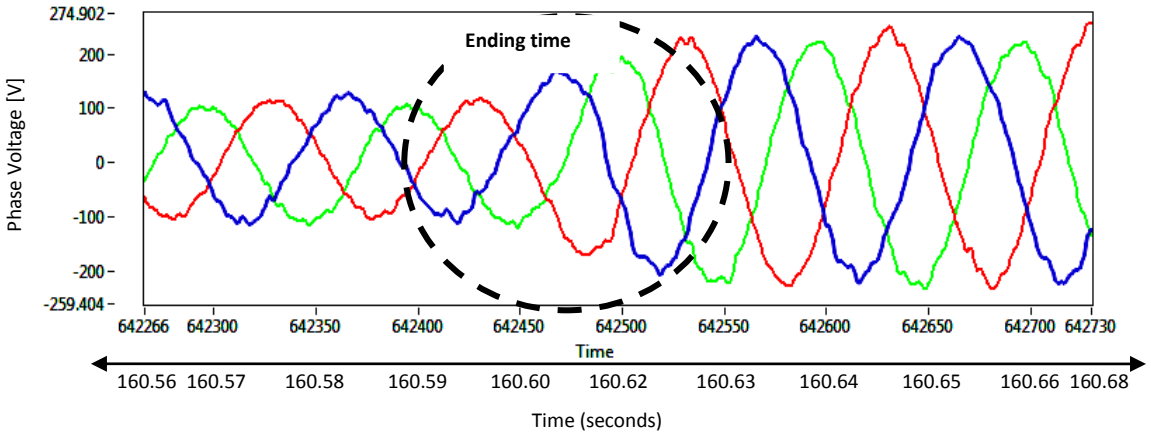


Figure 8.8: End of the Type-A Dip Implemented

Oscilloscope plots of the output voltage is presented in the figure 8.9 below. Only two phases are shown, since it was a dual channel scope.

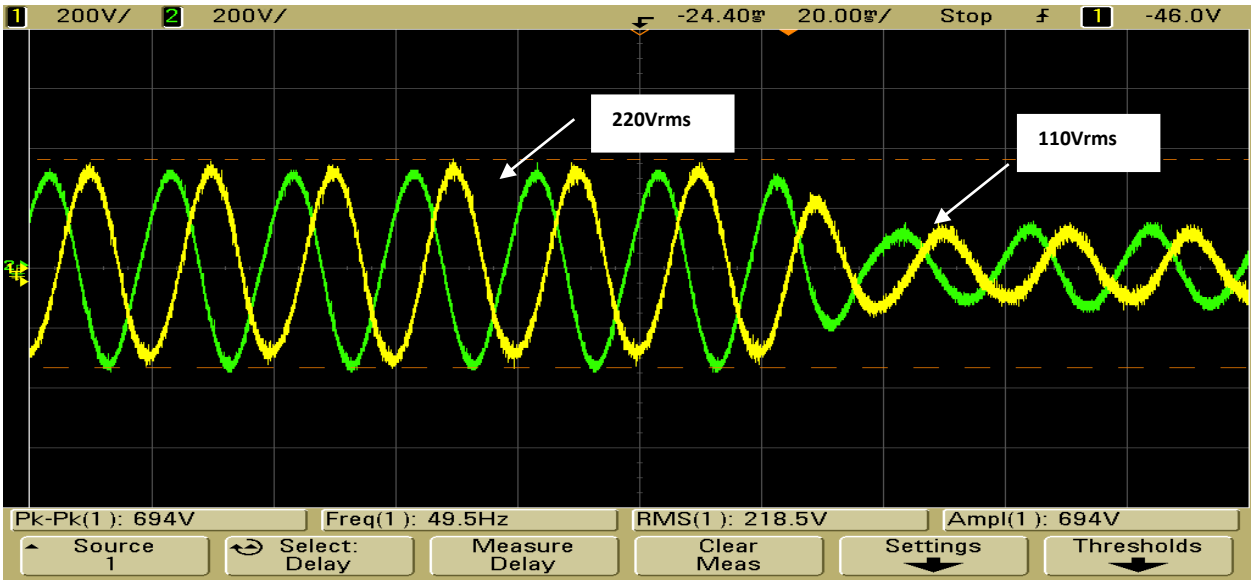


Figure 8.9: Scope Output of Type A Dip Implemented

For the analysis of the converters dynamic response, the three phase voltages are converted into *dq* components. Since Type A is a symmetrical dip, there will be no negative sequence component in this case, hence giving a certain values of direct and quadrature axis positive components. Per unit analysis is done for the *dq* components for the rest of the chapter. Positive *dq* reference frame components are shown in figure 8.10. 50% magnitude dip applied is shown in the waveform and can be verified from the figure 6.10.

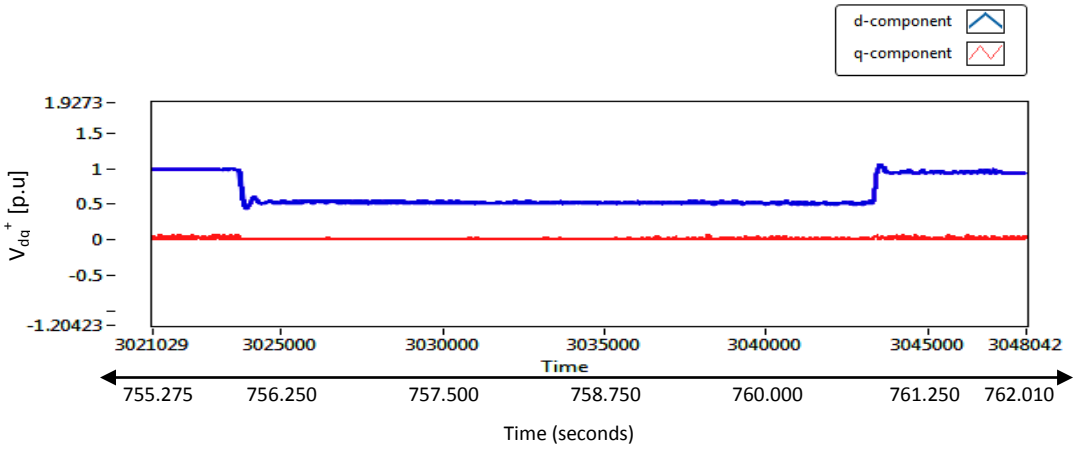


Figure 8.10: Positive *dq* Components of the Type A Dip Implemented

Zoomed-in screen shots of the *dq*-components are shown below.

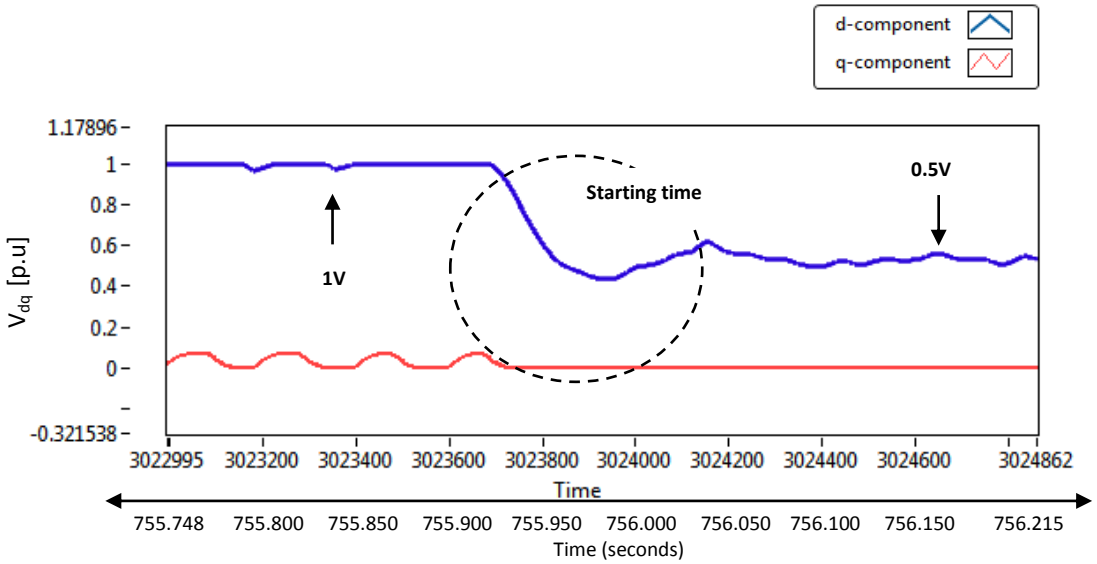


Figure 8.11: Start of the Positive *dq* Components of Type A Dip

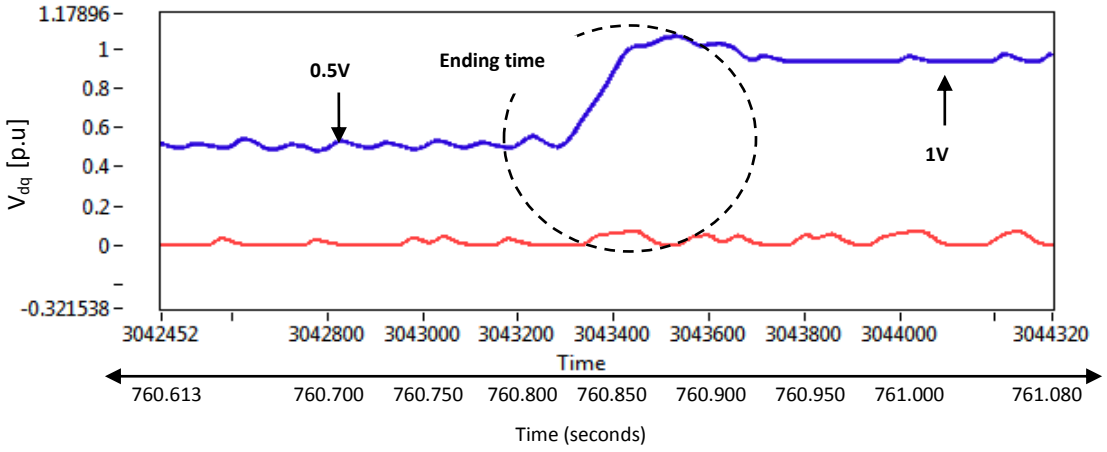


Figure 8.12: End of the Positive *dq* Components of Type A Dip

Figure 8.11 and 8.12 show the settling time of 50ms at the start and 40ms at the end of the dip.

➢ Type B Dip

The type B was introduced to the system by again changing the voltage reference values. It reduces the magnitude on one phase while maintaining the other two at the nominal value. The phase angles are maintained at 120° thereby allowing magnitude unbalance to be implemented as shown in figure 6.12. Figure 8.13 shows the waveforms in which a single phase

(B) has a lower magnitude than the other two. Slight deviations in magnitude of phases A and C voltages can be seen from the nominal value. This phenomenon is explained in [47] where voltage dip is described in terms of segments. This segmentation has five different types as mentioned below

- Pre-Event Segment
- First Transition Segment
- During Event Segment
- Second Transition Segment
- Voltage Recovery Segment

Here a second transition can be seen in figure 8.13 where the voltage abruptly changes to more than the nominal voltage magnitude.

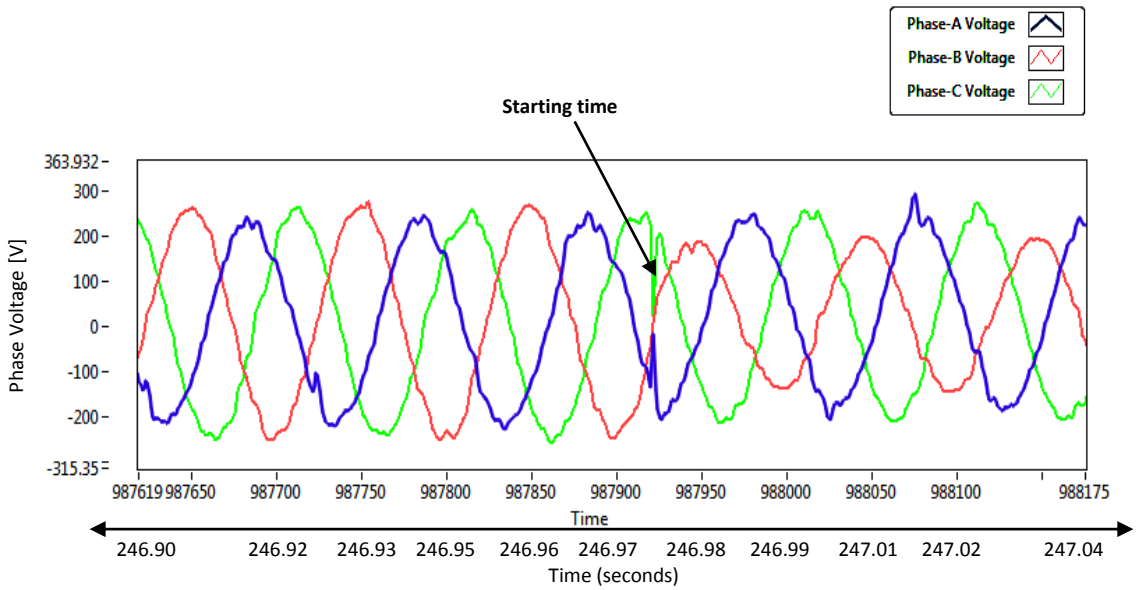


Figure 8.13: Start of the Type B Dip Implemented

A 50% voltage dip was implemented. The start and end time of the dip are shown in the figures 8.13 and 8.14. The figures show correlation with figure 6.14.

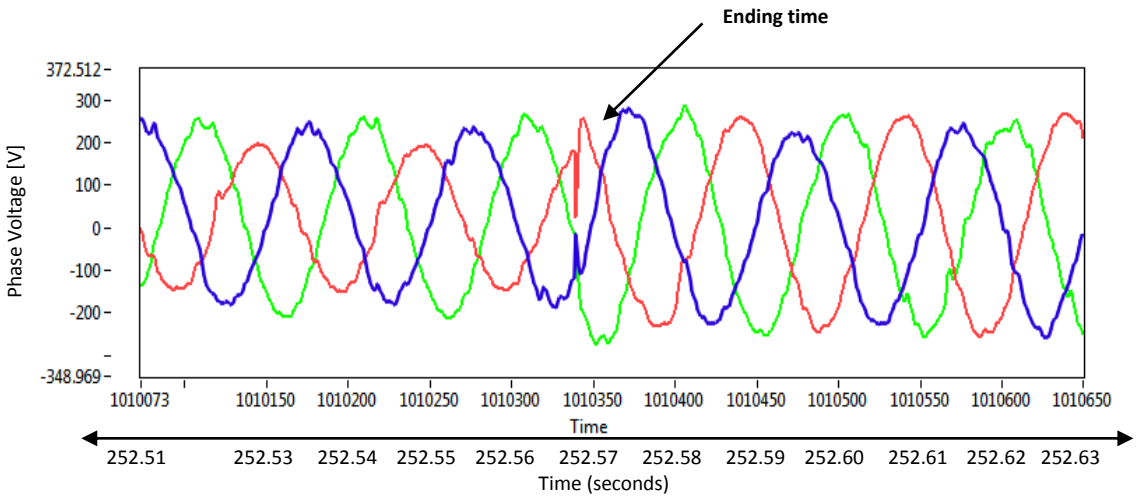


Figure 8.14: End of the Type-B Dip Implemented

The experimental results were further verified by means of a power quality analyzer. The analyzer was attached to the output of the emulator and the waveforms on its screen are presented below in the figure 8.15.

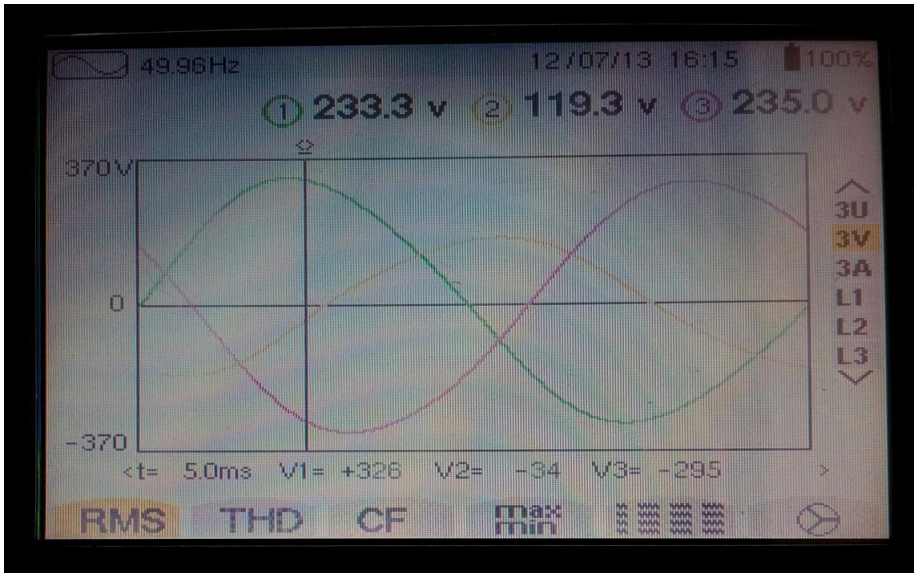


Figure 8.15: Type-B Dip from the Analyzer Output

With reference to figure 8.15 a single phase with less magnitude can be seen. The waveforms were automatically smoothed by the analyzer. THD was also checked and is illustrated below.

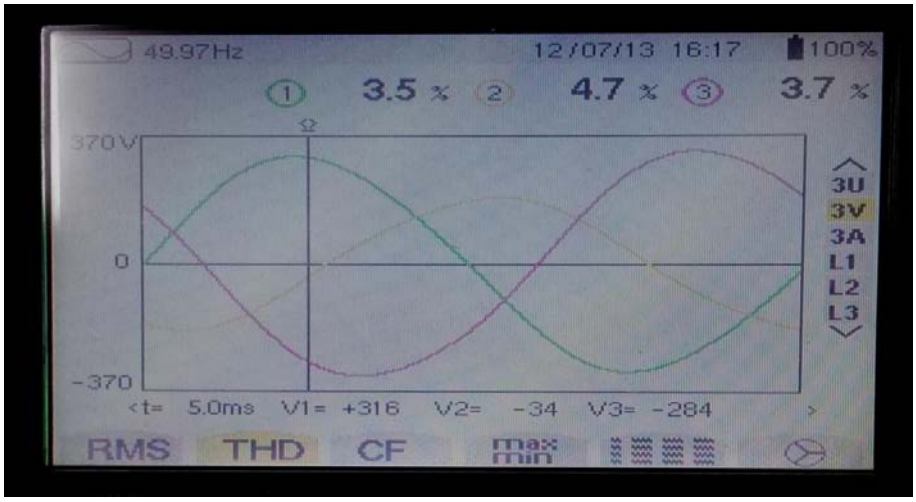


Figure 8.16: Percentage THD of the Type-B Dip from the Analyzer Output

Phase unbalance during the Type B dip occurred unexpectedly and is shown in the figure 8.17 below. For a perfectly balanced system the angle between phases should be 120°, but in this instance it was 105° and 150° respectively.

The following results could be one of the reasons for phase unbalance [48][49]:

- Change of during dip magnitude is often associated with phase unbalance.
- In-line inductance can introduce phase unbalance.
- Unbalanced load can bring during-dip phase unbalance.

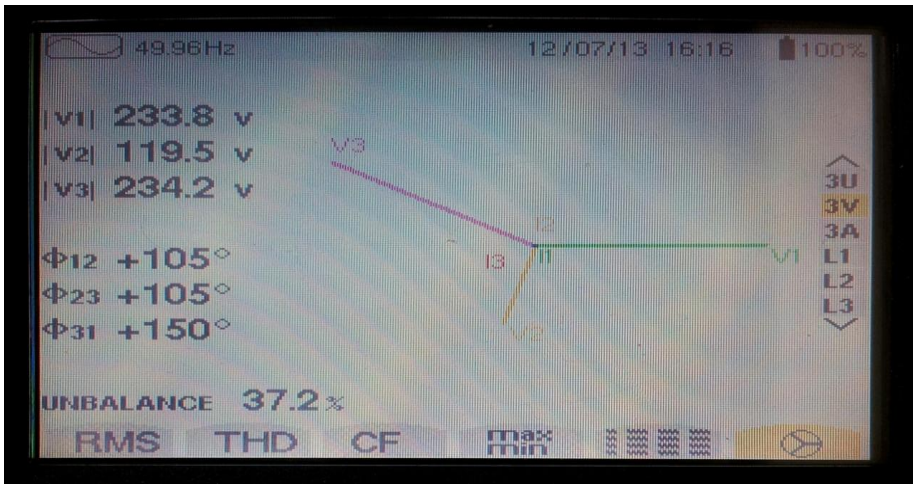


Figure 8.17: Phase Information of the Type-B Dip from the Analyzer Output

With reference to figure 8.17 it could be concluded that there was a slight phase unbalance in the output waveforms and needs further work to improve it. From [50] true definition of voltage unbalance calculation can be applied to calculate the percentage phase voltage unbalance rate.

$$\%PVUR = \frac{\max voltage\ deviation\ from\ the\ avg\ line\ voltage}{avg\ line\ voltage}.100 \qquad (8.1)$$

The three phase voltages are then converted into *dq* components. As this is an unsymmetrical dip a negative sequence component also appears in the *dq* rotating reference frame. Dual vector control explained in chapter 5 was then applied to control the positive and negative sequence voltage components. Figures 8.18 and 8.21 show the experimental results of positive and negative sequence *dq* voltages under the unbalanced condition. The controller performed as expected for the required unbalance set points. Again the comparison is made between percentage magnitude deviation and the waveform spectrum quality. IEC power quality standards of voltage dips are then applied for residual voltage calculation as discussed in chapter 6.

Figure 8.18 shows the positive sequence components. A 50% dip on one phase was applied which led to a 20% magnitude deviation, calculated from the discussion in figure 6.15. For a 50% balanced voltage dip the waveform should go to the half of the peak voltage i.e 0.5V but here the positive sequence *d*-component only went down to 0.7V. Here the residual voltage generated 0.2V of magnitude deviation whereas the q-component stayed at zero.

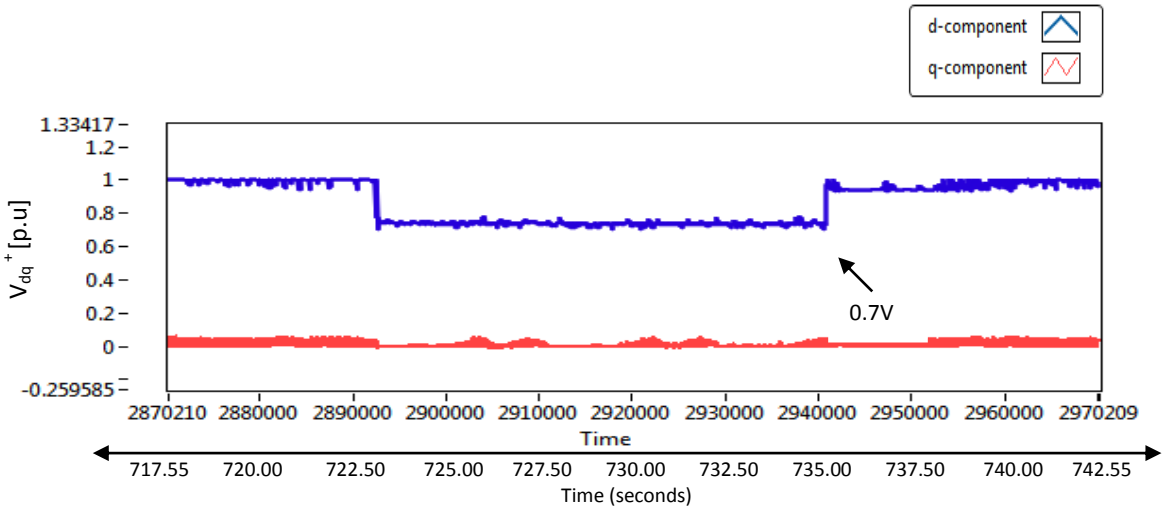


Figure 8.18: Positive *dq* Components of the Type B Dip Implemented

Figure 8.18 shows a correlation with figure 6.16 with 10% less deviation. The dynamic response of the converter can be analysed from the following zoomed-in screen shots of the figure 8.18 :

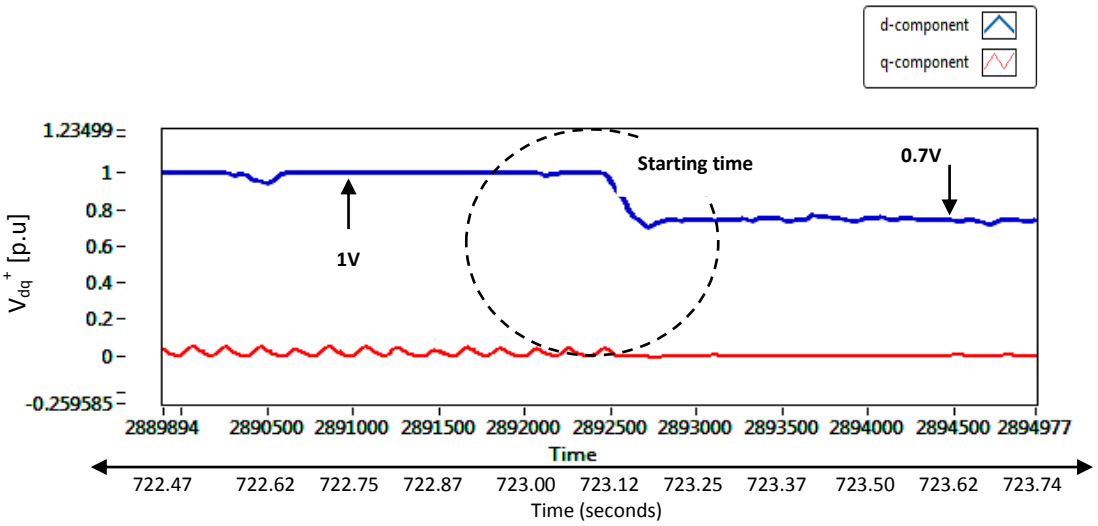


Figure 8.19: Start of the Positive *dq* Components of Type B Dip

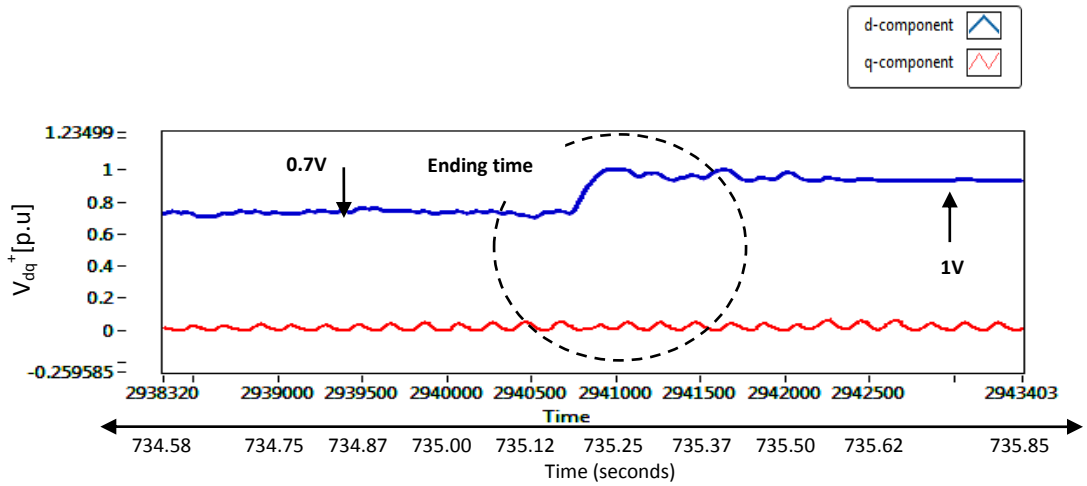


Figure 8.20: End of the Positive *dq* Components of Type B Dip

Figures 8.19 and 8.20 show a settling time of 80ms at the start and 50ms at the end of the dip. Similarly, in figure 8.21 the negative *d*-component should remain at zero during the symmetrical dip but here it increases to 0.28V, which is the residual voltage itself. Thereby, generating 28% of magnitude deviation on the *d*-component and 5% on the *q*-component respectively. Figure 8.21 shows correlation with figure 6.17.

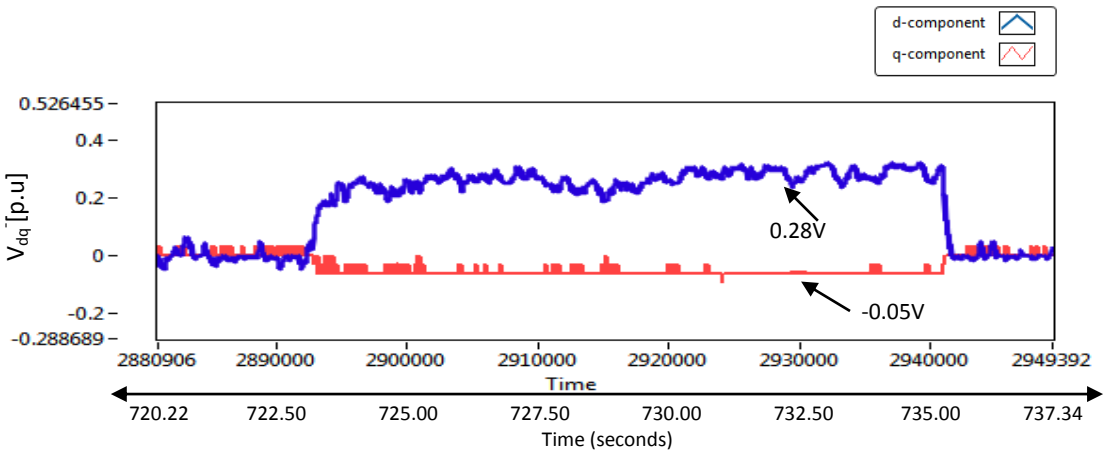


Figure 8.21: Negative *dq* components of the Type B Dip Implemented

The above figure has a certain amount of ripple in it. As discussed in section 4.4.1, the transformation equation 4.18 can be further expanded which clearly shows the AC part of the negative sequence component.

$$v_{dq}^{-} = e^{-J\Theta}.v_{\alpha\beta} \qquad [8.2]$$

$$= \begin{bmatrix} v_d^- \\ v_q^- \end{bmatrix} + \begin{bmatrix} v_d^+ \cos(\theta^- - \theta^+) + & v_q^+ \sin(\theta^- - \theta^+) \\ -v_d^+ \sin(\theta^- - \theta^+) + & v_q^+ \cos(\theta^- - \theta^+) \end{bmatrix} \qquad [8.3]$$

$$= \underbrace{v_{dq}^{-}}_{\text{DC term}} + \underbrace{e^{-J(\theta^- - \theta^+)}.v_{dq}^{+}}_{\text{AC term}} \qquad [8.4]$$

This AC term constitutes ripple in the waveform. Dynamic response of the converter can be analysed by considering zoomed-in screen shots of the above figure 8.21:

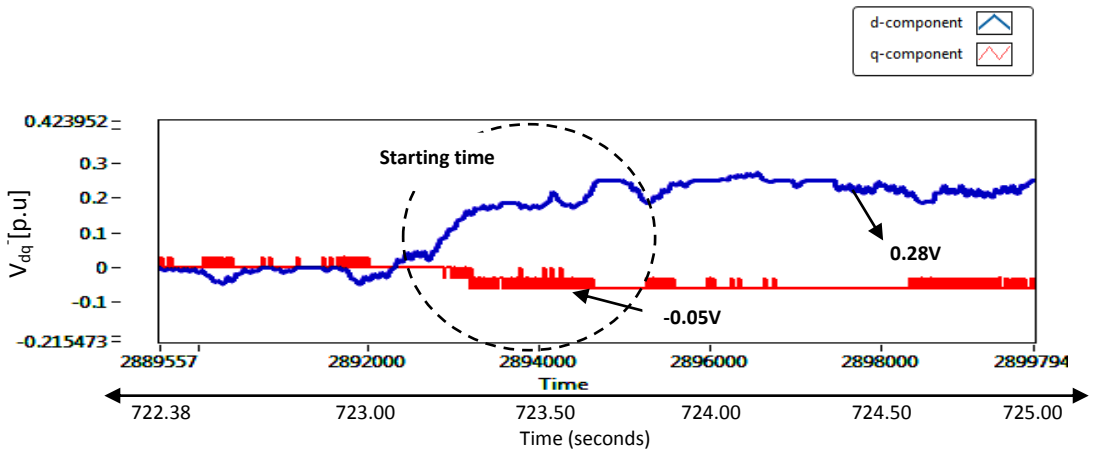


Figure 8.22: Start of the Negative *dq* Components of Type B Dip

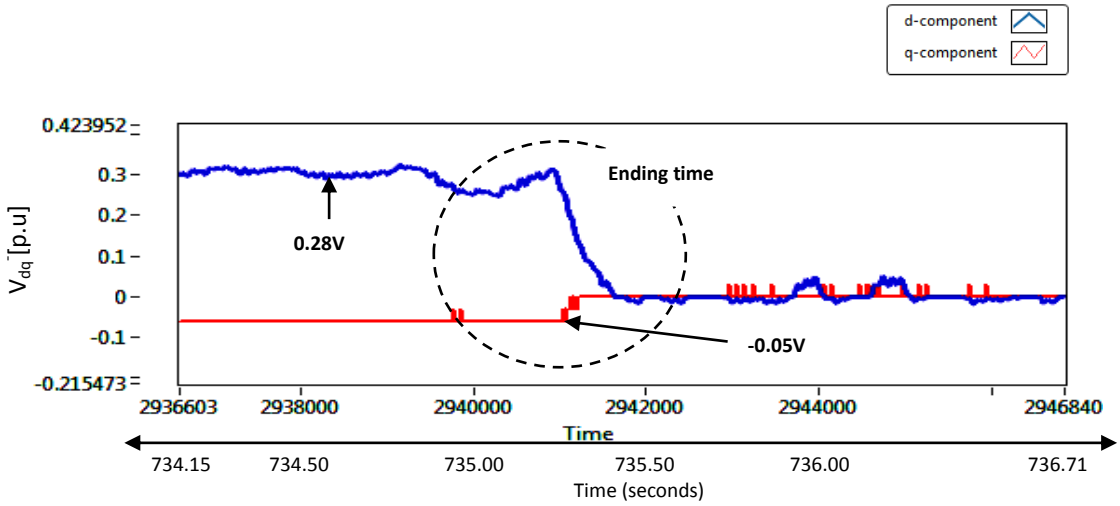


Figure 8.23: End of the Negative *dq* Components of Type B Dip

Figure 8.22 and 8.23 show a settling time of almost 250ms at both start and end of the dip. The results in the above figures can be correlated to the simulation figure 6.17. A slight deviation in negative *d*-component was also recorded which could be the source for waveform distortion and slow control response.

➢ Type E Dip

This dip reduces the magnitude on two phases while maintaining the third at nominal voltage. The phase angles are maintained thereby allowing magnitude unbalance to be implemented as shown in chapter6, figure 6.18. Figure 8.24 shows the waveforms in which two phases have a

lower magnitude than the third. The change in magnitude on phases A and C voltage can be seen.

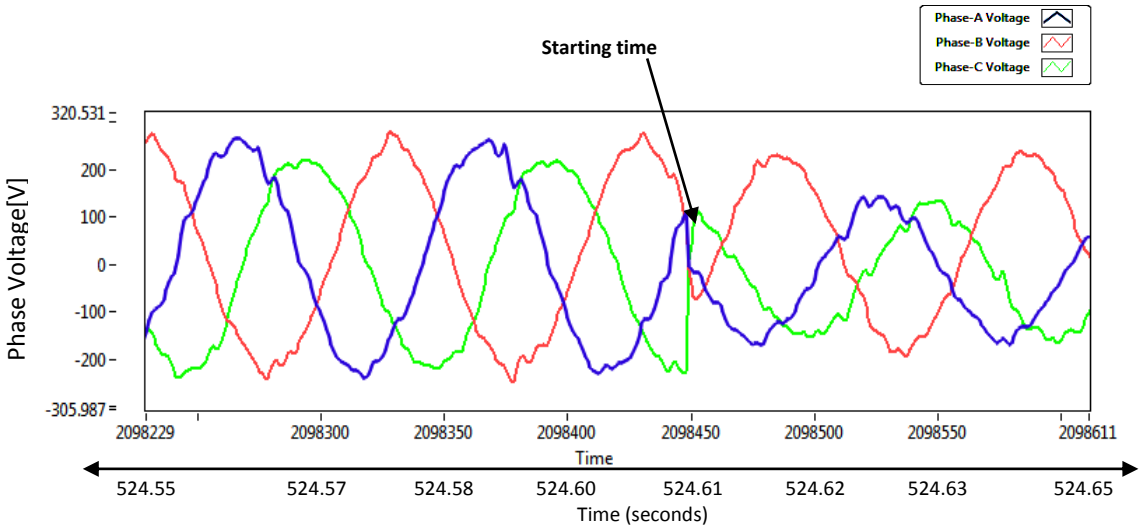


Figure 8.24: Start of the Type E Dip Implemented

The start and end time of the 50% dip on two phases are shown in the figures 8.24 and 8.25 respectively. The figures show correlation with the waveforms in figure 6.20.

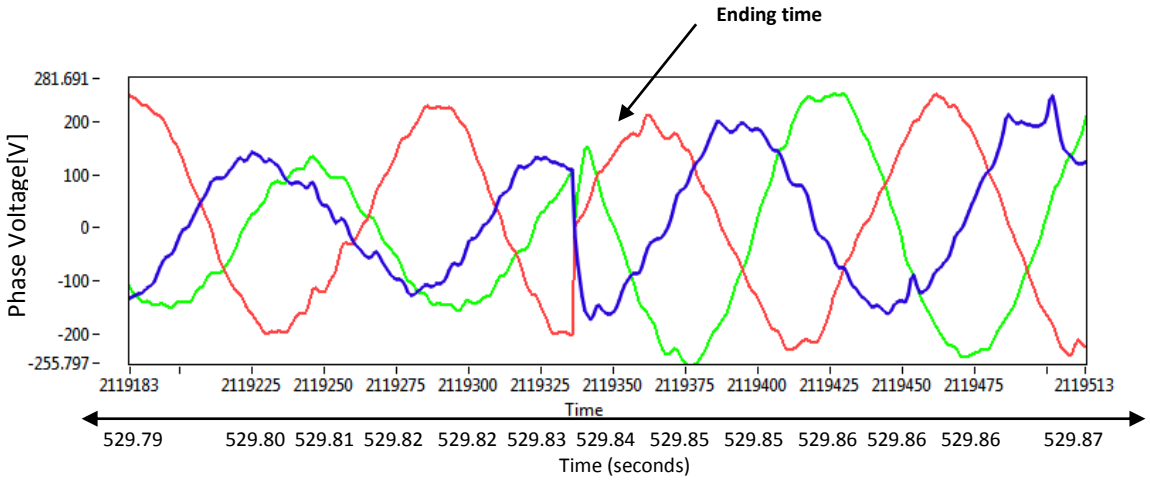


Figure 8.25: End of the Type-E Dip Implemented

The experimental implementation of the Type-E dip can be further verified. A power quality analyzer was attached to the phase voltage output waveforms of the emulator and are shown below.

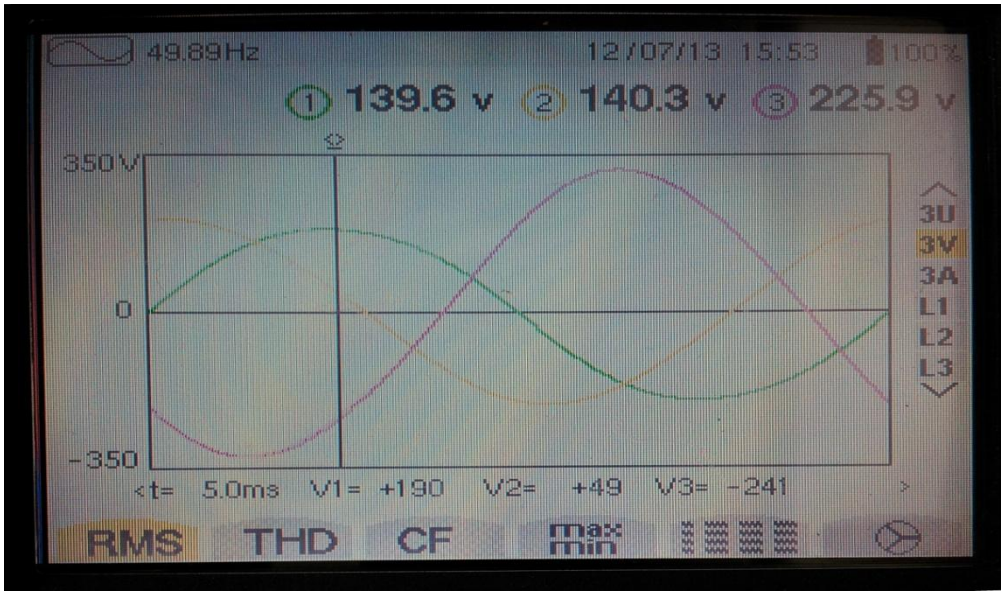


Figure 8.26: Type-E Dip from the Analyzer Output

As discussed earlier an unexpected phase unbalance was recorded which is shown in the figure below. For a perfectly balanced system the in-phase angle should be 120° but here it is -73° and -143° respectively.

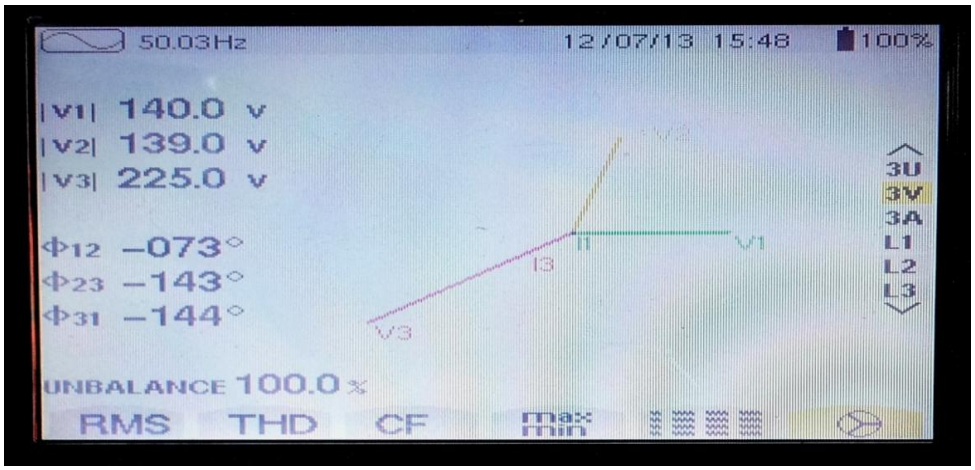


Figure 8.27: Phase Information of the Type-E Dip from the Analyzer Output

From section [8.3] the true definition of voltage unbalance can be applied to calculate the percentage unbalance factor.

The three phase voltages are then converted into *dq* components. Figure 8.28 and 8.31 show the experimental results of positive and negative sequence *dq* voltages for this unbalanced condition. Figure 8.28 shows the positive sequence components. It can be seen from the figure that a 50% dip on two phases was applied which led to a 5% magnitude deviation. For a 50% symmetrical voltage dip the waveform goes to half of the peak voltage i.e 0.5V. However, here the positive sequence *d*-component only dropped to 0.55V, which is the residual voltage generating 0.05V of magnitude deviation and the *q*-component stayed at zero. Moreover, it is noticed from the figure 8.18 and 8.28 that the positive *d*-component in the Type-E dip has lower magnitude deviation than the positive d-component of the Type-B dip. From the results it is recorded to be 15%.

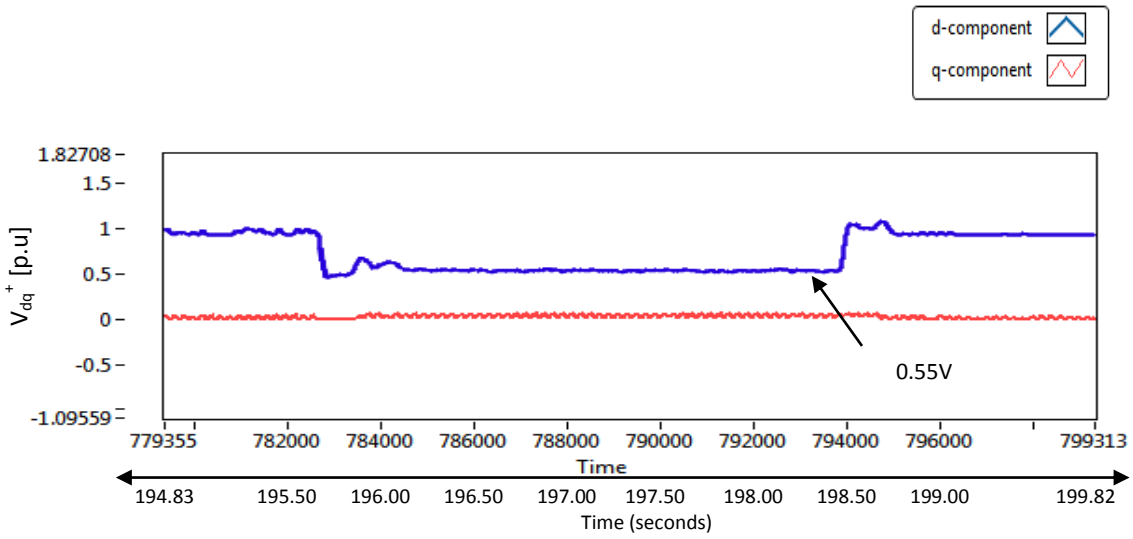


Figure 8.28: Positive *dq* Components of the Type E Dip Implemented

Figure 8.28 shows correlation with figure 6.21. The dynamic response of the converter can be analysed by considering the zoomed-in screen shots of figure 8.28:

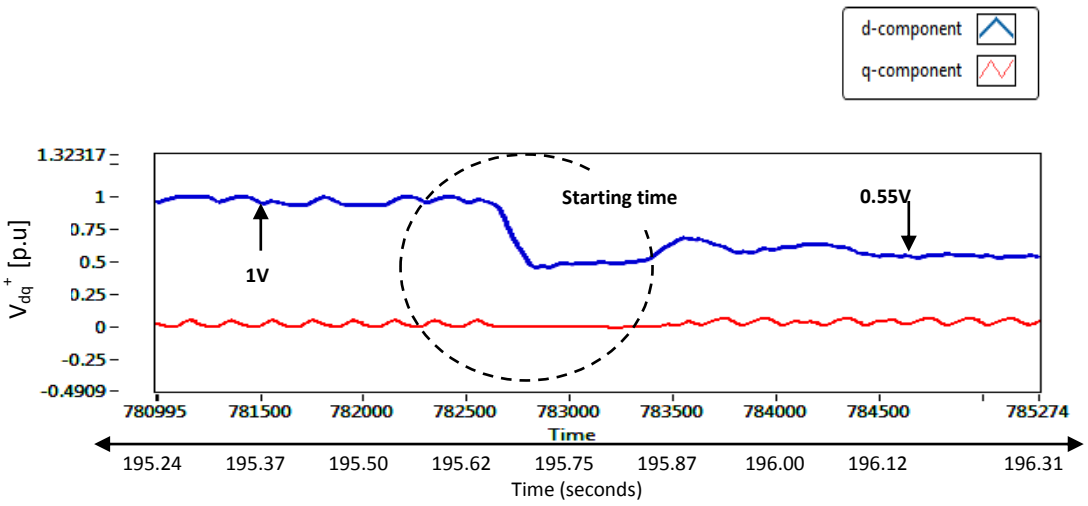


Figure 8.29: Start of the Positive *dq* Components of Type E Dip

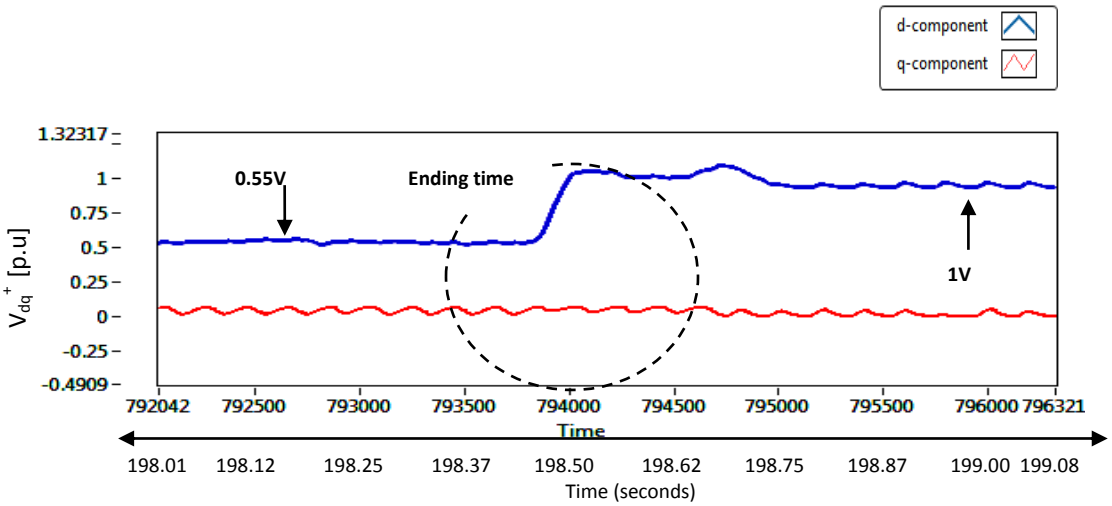


Figure 8.30: End of the Positive *dq* Components of Type E Dip

Figures 8.29 and 8.30 show settling times of 90ms at the start and 75ms at the end of the dip. Similarly in figure 8.31 the negative sequence *d*-component for a balanced condition or a symmetrical dip remains at zero. However, here it reaches -0.9V which is the residual voltage itself. Thereby generating 90% of magnitude deviation and *q*-component has 5% of deviation respectively. The negative value for the *d*-component was expected from the voltage transformation equations and from the simulations.

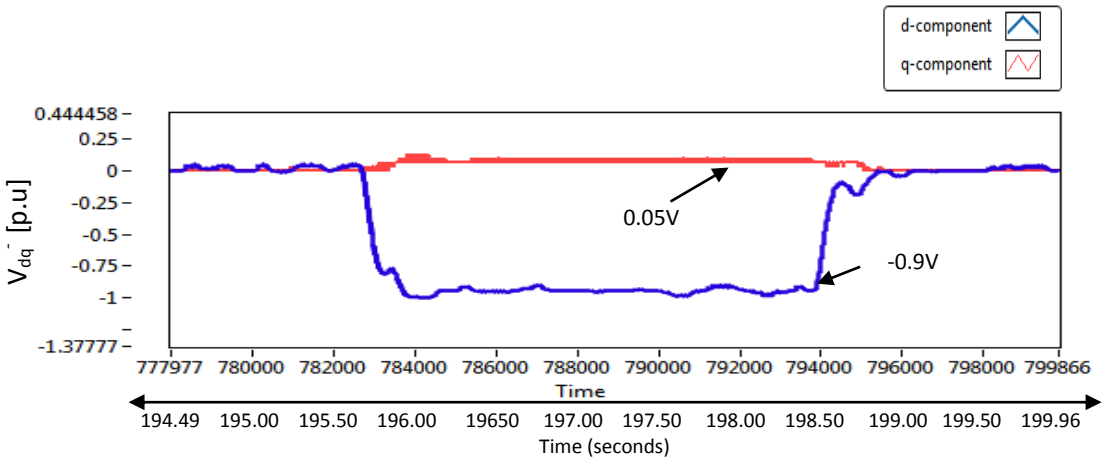


Figure 8.31: Negative *dq* Components of the Type E Dip implemented

The dynamic response for the negative sequence of the converter can be analysed from the following zoomed-in screen shots of the figure 8.31 above:

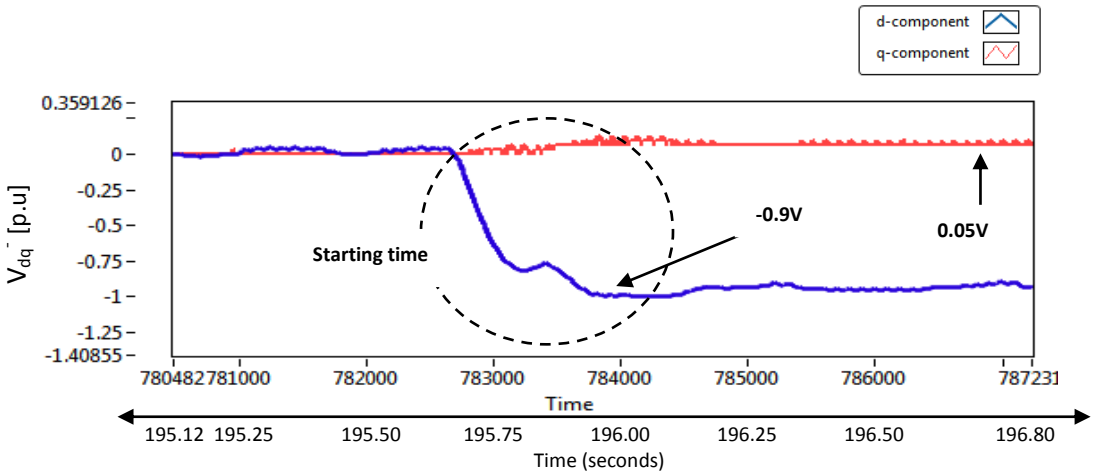


Figure 8.32: Start of the Negative *dq* components of Type E Dip

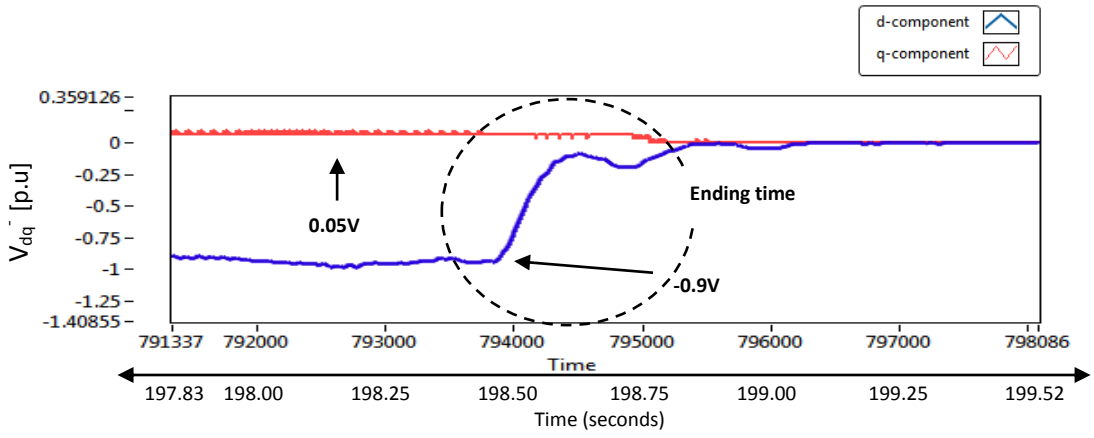


Figure 8.33: End of the Negative *dq* components of Type E Dip

Figure 8.32 and 8.33 show a settling time of 160ms at the start and 140ms at the end of the dip. It can be concluded that the Type-E dip has a high negative *d*-component deviation in comparison with the Type-B dip negative *d*-component and it was 65%. Moreover, the average dynamic response of the converter for all the positive sequence responses is 75ms, whereas for negative sequences it is approximately 200ms.

8.2.3.2. Voltage Swell/Overvoltage

This is a momentary increase of the voltage, beyond the normal tolerances, for more than one cycle and typically less than a few seconds. Thus resulting magnitude increase on all three phases but the phase angles are maintained, thereby allowing symmetrical magnitude change to be implemented as shown in figure 8.34. In the figure below a 50% symmetrical overvoltage is implemented on the grid emulator's output.

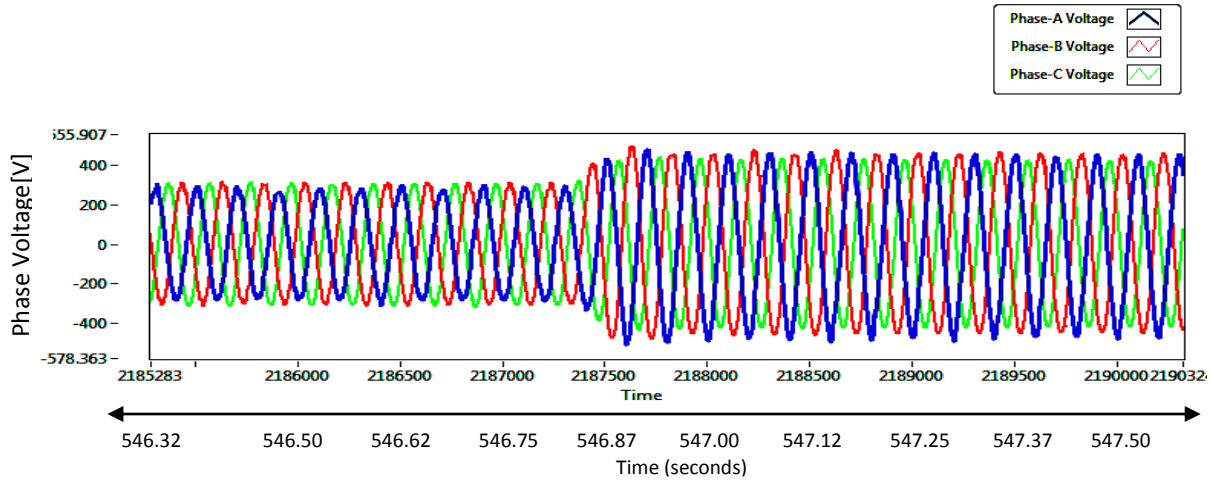
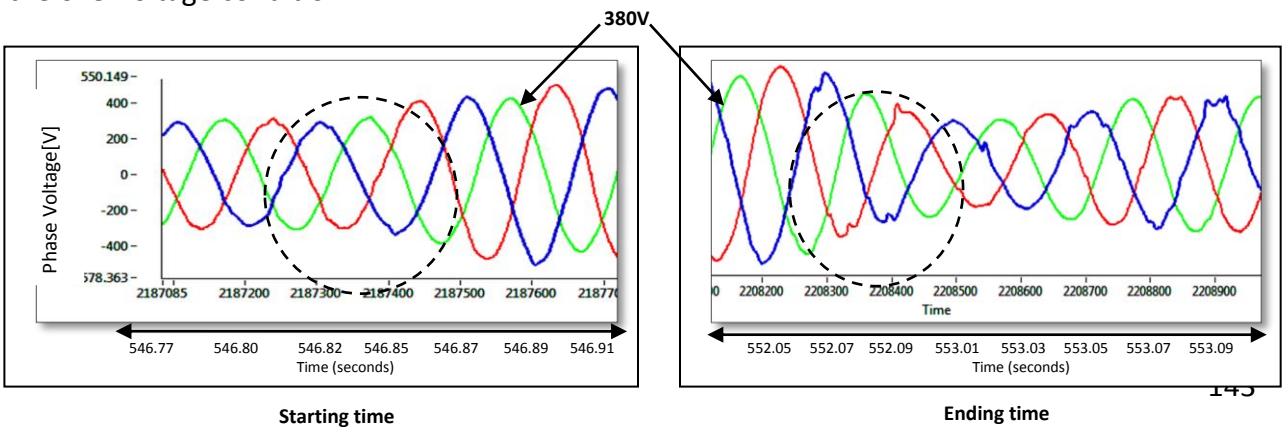


Figure 8.34: Symmetrical Overvoltage Implemented

Zoomed-in screen shots are shown below in figure 8.35 which illustrates the start and end of the overvoltage condition.



Starting time **Ending time**

Figure 8.35: Zoomed-in Screen Shots of the Overvoltage Implemented

In order to analyse the dynamic response, the three phase voltages are converted into *dq* components. A 50% overvoltage is applied from the grid emulator. As it is a symmetrical overvoltage, there will be no negative sequence *dq*-component. The positive *dq* waveforms are shown in figure 8.36.

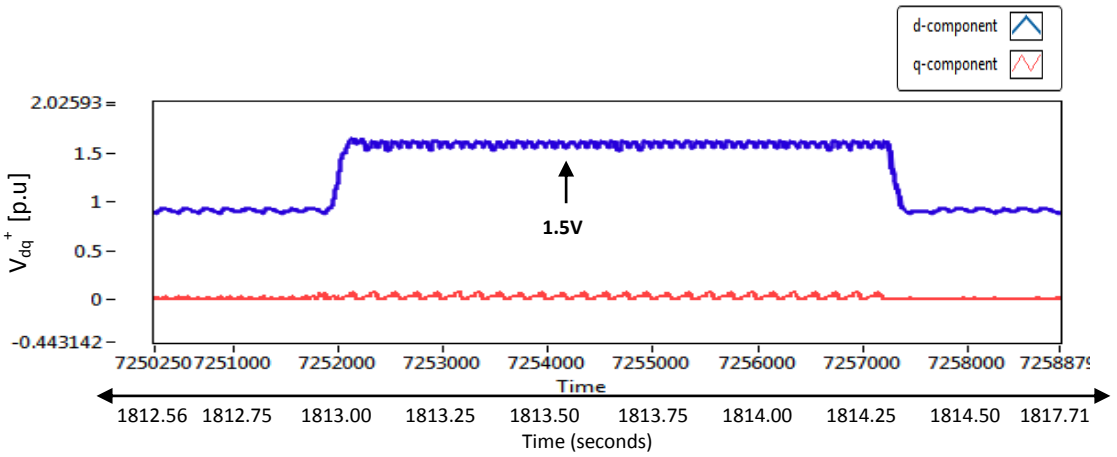


Figure 8.36: Positive *dq* components of the Symmetrical Overvoltage Implemented

Zoomed-in screen shots for the start and end of the overvoltage condition are shown below. Figure 8.37 shows the settling time for the overvoltage, which is approximately 90ms for both cases.

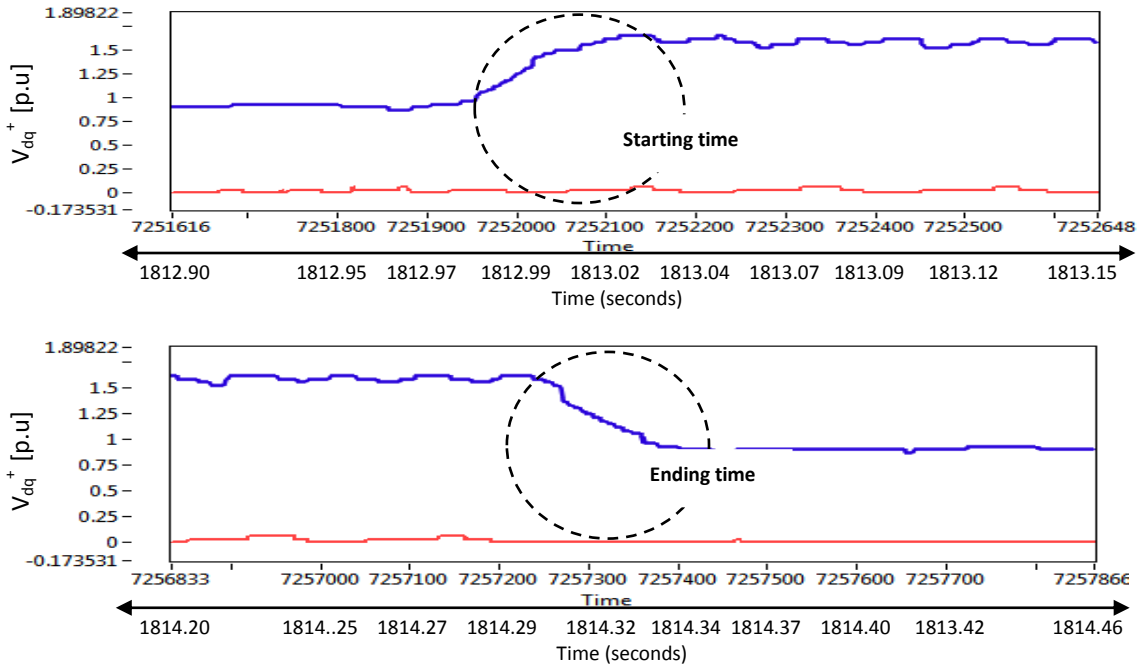


Figure 8.37: Zoomed-in Screen Shots of the Positive *dq* Components

A comparison of the dynamic response for both converters is done at the end of this chapter.

8.3. Three-level Converter

The performance of the three level converter was analyzed experimentally. The same process was followed as for the two-level converter. The three-level converter was first tested as a grid-side converter (rectifier mode of operation) to control the DC link voltage whilst coupled to the two-level converter on the load side. It was then tested as a load-side converter (in inverter mode of operation) and connected to the DC-link, which was controlled by the two-level converter as discussed in section 6.1. The SVPWM technique of the three-level converter was used to control its switches as discussed in chapter 3. The PWM switching signals were developed in the Labview environment was then applied to the converter through the FPGA hardware mentioned in chapter 7. The output waveforms were then analysed in a Labview scope window and on an oscilloscope.

8.3.1. PWM Switching Signals of the Three-Level Converter

Line-to-neutral PWM switching waveforms of the three-level converter was analysed on an oscilloscope and are shown in figure 8.38. The filtered line-to-neutral PWM waveform which shows the fundamental line-to-neutral waveform is also shown. In the figure below, three voltage levels can be seen in the line-to-neutral voltage waveforms as discussed in chapter 3. For each half cycle two steps are missing (flattened) in the PWM output waveform. The reason could be the over-modulation of switching events or misplacement of the rotating vector and can be looked up for later modifications. However, it does not have any serious impact on the whole system's performance.

Figure 8.38: Van Line-to-Neutral Before Filtering and Vbn Output Voltage

8.3.2. Active Rectification Mode of Operation

The experimental tests performed on the three-level converter were implemented to control the DC link voltage. A VOC was applied with the help of SVPWM to achieve a stable DC link voltage in rectifier mode of operation. The dynamic response of the converter was tested to confirm the correct operation of the system.

The dynamic response of the three-level converter in rectifier mode was analysed. A step change in the DC link voltage results in proportional change to the grid current. Figure 8.39 below shows a steady state DC link voltage and the reference dynamic response of the converter. The dynamic response can be assessed by introducing a step in the reference of the DC link voltage. When the set point was changed from 350V to 160V and then 160V to 350V, figure 8.39 indicates a settling time of 0.50s in both cases.

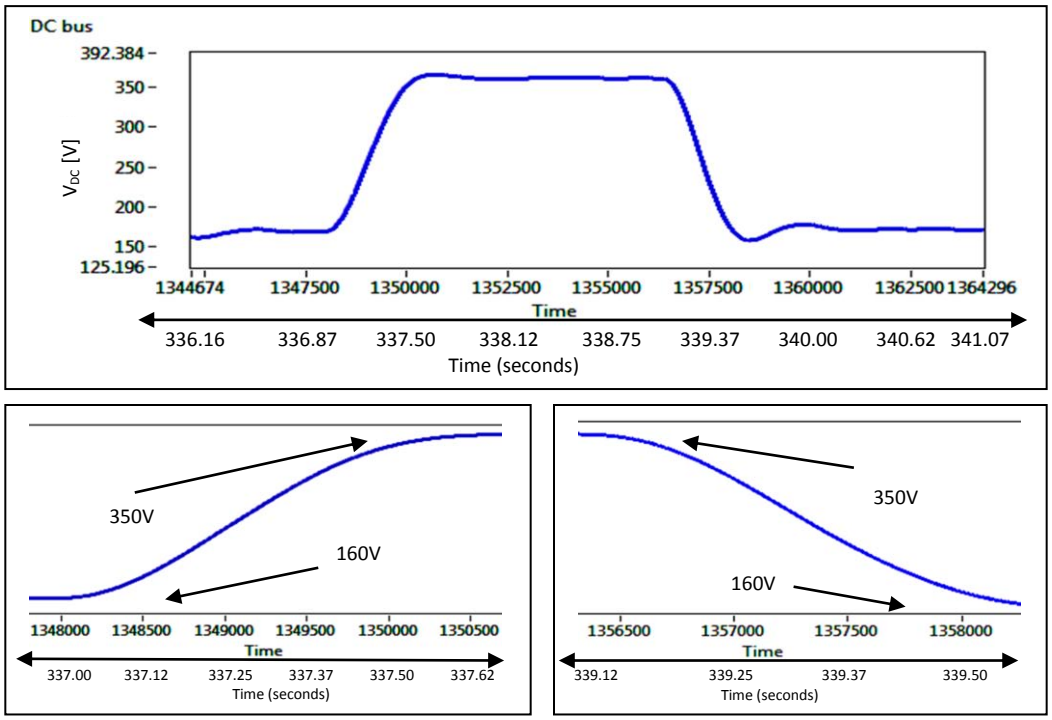


Figure 8.39: DC link Voltage Step

The effect of the step change in the DC-link voltage on the input grid current is shown in figure 8.40. The change in the grid currents can be seen on the same instances when the DC link

voltage step was applied. For a constant impedance load across the DC link, the increase in V_{DC} should correspond to a slight boost in current on the grid side.

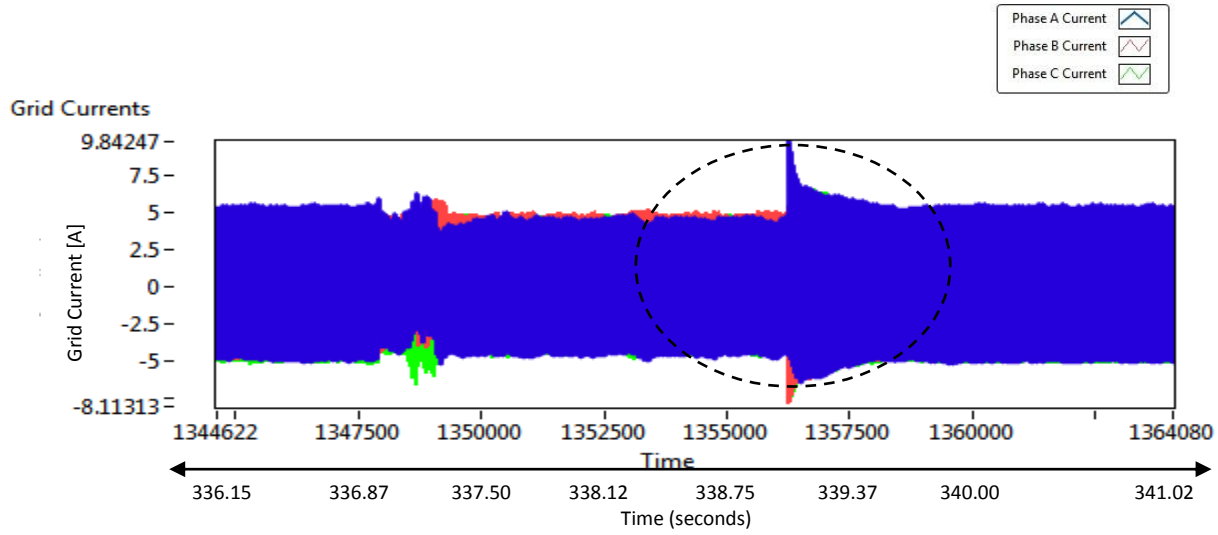


Figure 8.40: Grid current Affected by DC Link Voltage Step

Zoomed in screen shot of the current to the step change in the DC link voltage is shown in the figure below :

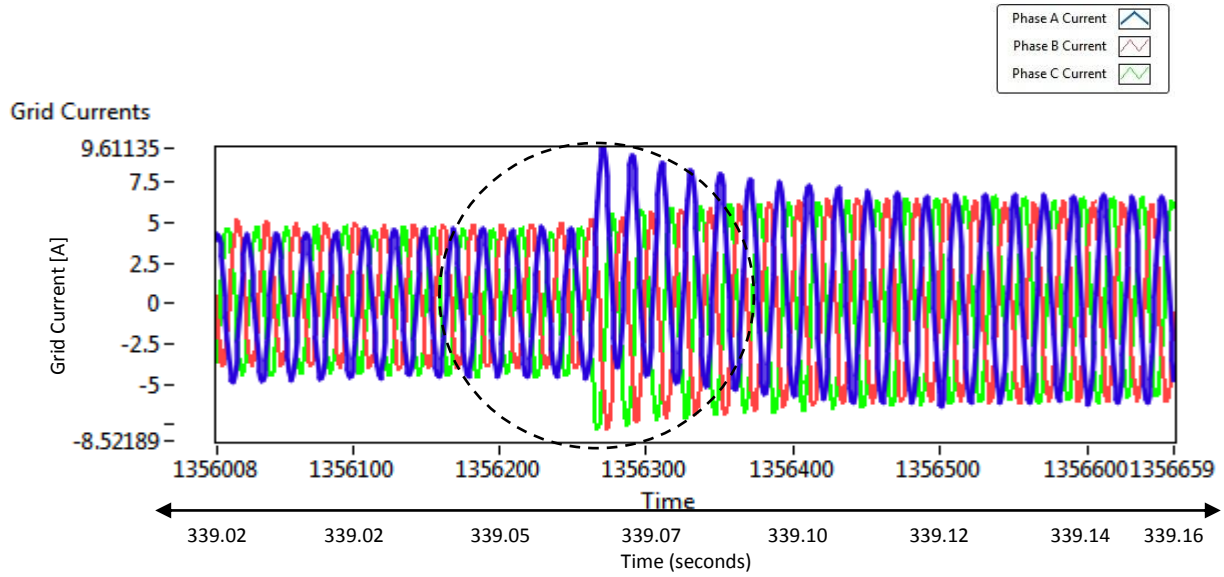


Figure 8.41: Zoomed-in Grid Current Affected by DC Link Voltage Step

It is to be noted from figures 8.3 and 8.39 that for the three-level converter step response for the DC link voltage is bit faster and with less distortion as compared to the two-level converter.

8.3.3. Inverter Mode of Operation

In this section the three-level converter is operated in inverter mode and is connected to the DC link, which is controlled by the two-level converter. Under-voltage (dip) and over-voltage (swell) conditions are then applied. The performance of the converter is analysed in detail.

8.3.3.1. Voltage Sag/Voltage Dips

Type A, B and E dips are investigated for the three-level converter. A dual vector control was implemented in order to implement and control the dip on each phase, thereby creating the desired unbalance. The converter was loaded with a 1kW passive load during all the experiments.

- **Type A Dip**

  A type A dip was introduced by changing the voltage reference values as shown in figure 5.14. Experimental results which relate to the simulations conducted in section 6.1.3 are presented here. Figure 8.42 shows the measured output voltage of the emulator with a three-level converter in inverter mode of operation. The change in magnitude on all three phases can be seen for the Type A dip which was implemented.

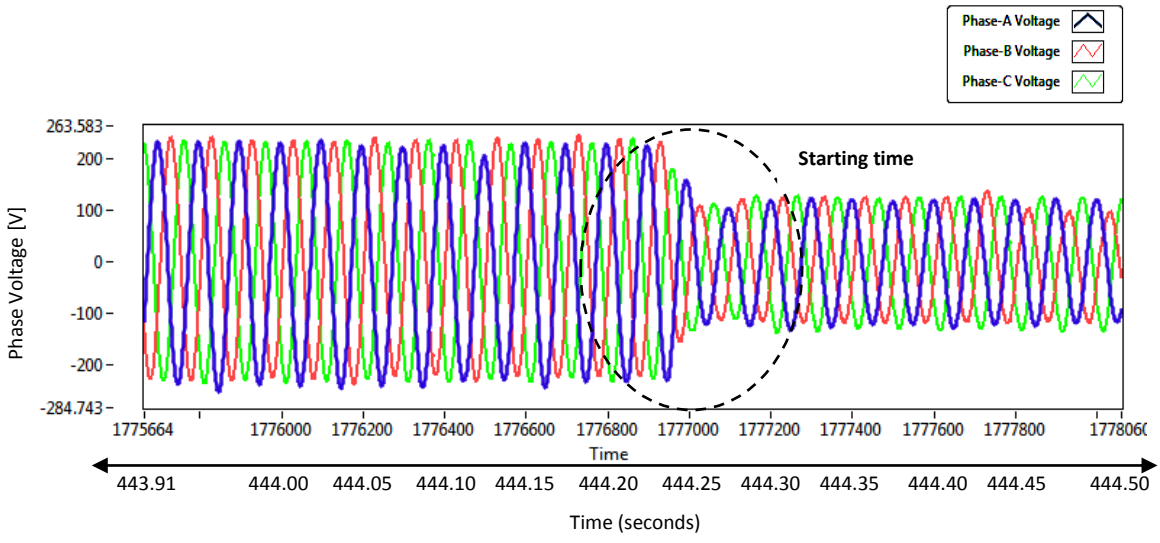


Figure 8.42: Start of Type A Dip Implemented

A symmetrical dip of 50% on all three phases is evident from the figure below. The start and end of the dip are shown in the figures 8.42 and 8.43. The figures show the same waveforms as illustrated in chapter 6, figures 6.30 and 6.31.

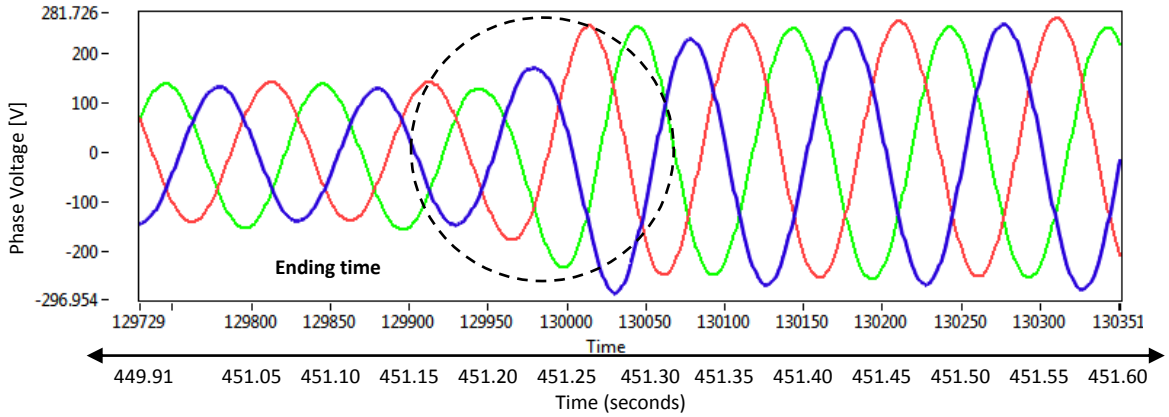


Figure 8.43: End of the Type-A Dip Implemented

By comparing figures 8.8 to figure 8.43 it can be seen that the output waveform of the three-level converter is much smoother than that of the two-level converter which was expected from the discussion in chapter 2 and 3. The voltage waveforms measured on an oscilloscope is presented below. Only two phases are shown due to the fact that a dual-channel oscilloscope was used.

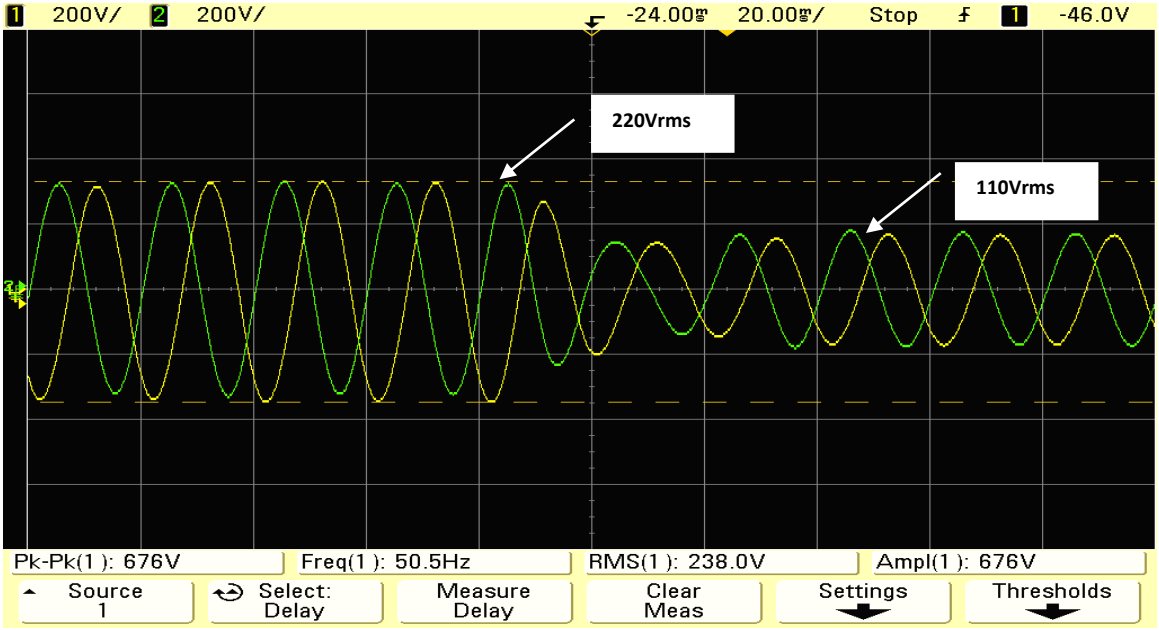


Figure 8.44: Scope Output of Type A Dip Implemented

For the analysis of the converters dynamic response, the three phase voltages are converted into *dq* components. As Type A is a symmetrical dip, there will be no negative sequence components. Furthermore the positive sequence quadrature axis component is zero due to the alignment of the d-axis with the output voltage phasor of the converter. The positive sequence *dq* waveforms are shown in figure 8.45. The waveforms resemble those achieved in simulations as shown in figure 6.32.

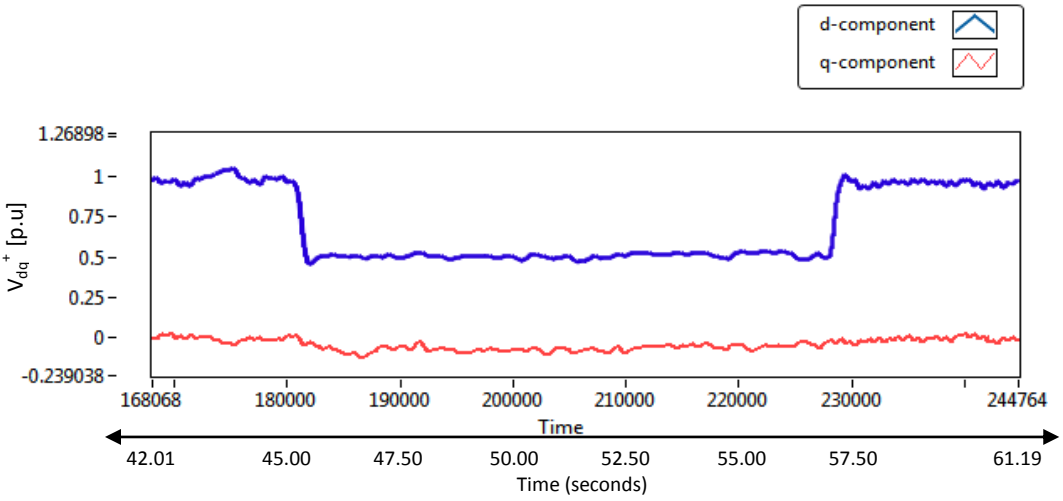


Figure 8.45: Positive *dq* components of the Type A Dip implemented

Zoomed-in screen shots of the *dq*-components for 50% Type A dip on all three phases are shown below.

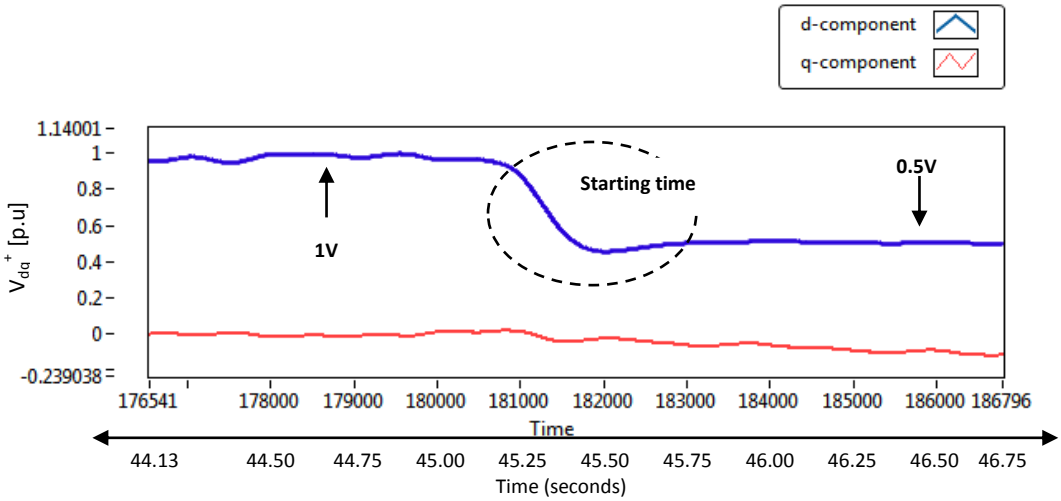


Figure 8.46: Start of the Positive *dq* components of Type A Dip

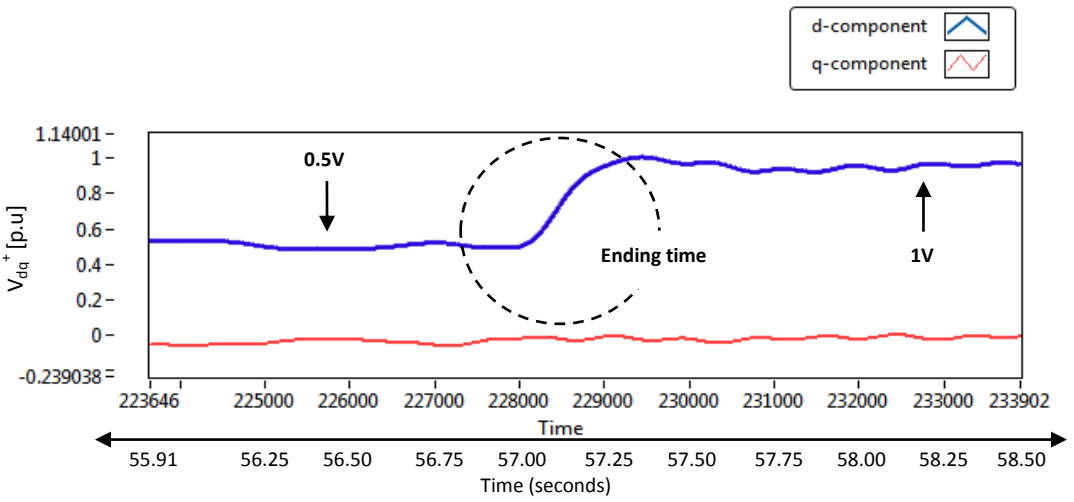


Figure 8.47: End of the Positive *dq* components of Type A

Figures 8.46 and 8.47 show the settling time of 150ms at the start and 200ms at the end of the dip.

➢ Type B Dip

A Type B dip was introduced to the system by again changing the Va, Vb & Vc reference values. Figure 8.48 shows the output voltage for a Type B dip where a single phase (A) has a lower magnitude than the other two. An unexpected deviation in magnitude on phases (B) and (C) voltage from the nominal value can also be seen due to the second transition segment, which is previously discussed for figure 8.13.

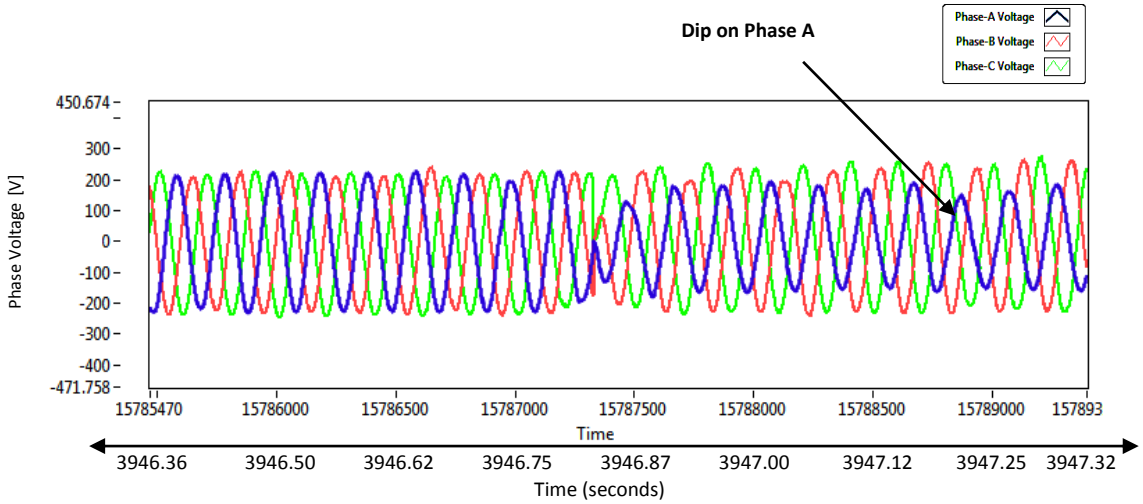


Figure 8.48: Type B Dip Implemented

A 50% voltage dip was implemented on phase A. The waveforms presented in figure 8.48 correlates with the simulated dip in figure 6.34. Experimental results can be further analyzed by means of the power quality analyzer's output voltage waveforms connected to the emulator's output, type-B dip is presented below.

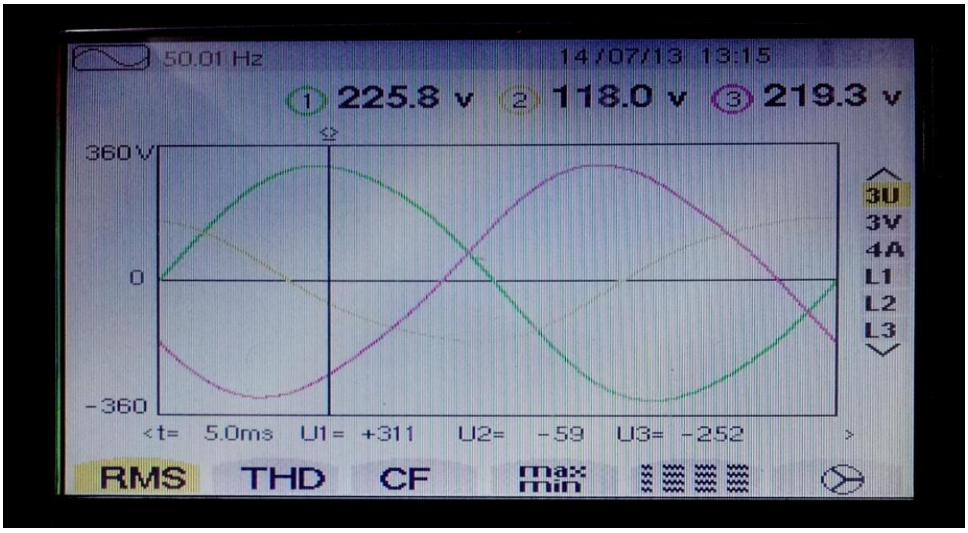


Figure 8.49: Type-B Dip from the Analyzer Output

A single phase with 50% of the nominal magnitude can be seen. THD was also checked and is shown below. By comparing figure 8.16 and 8.50 it can be seen that the waveform presented for three-level converter has lower THD.

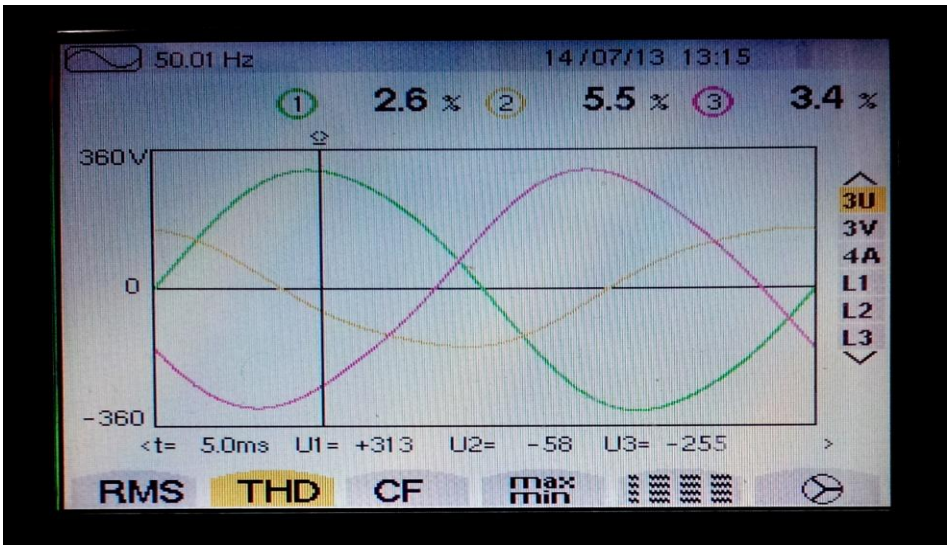


Figure 8.50: Percentage THD for the Type-B Dip from the Analyzer Output

An unexpected phase unbalance occurred in the waveform and is shown in figure 8.51. For perfectly balanced system the in-phase angle should be 120° but here it is -108°, -102°and -150° respectively.

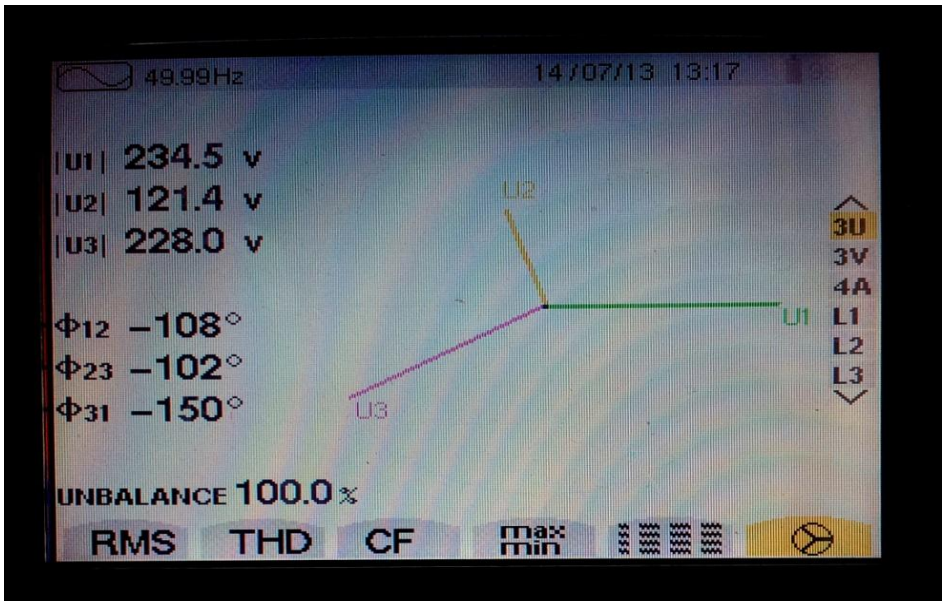


Figure 8.51: Phase Information for the Type-B Dip from the Analyzer Output

The three phase voltages are then converted into *dq* components in order to analyze the dynamics of the converter with this dip. Since this is an unsymmetrical dip negative sequence components also appears in the *dq* reference frame due to the unbalance present in the three-phase output of the converter. Dual vector control explained in chapter 5 was then applied to control the negative sequence voltage. Figure 8.52 shows the positive sequence components. A 50% dip on one phase was applied, which led to a 15% magnitude deviation. For a 50% balanced voltage dip the waveform should reduce to the half of the peak voltage i.e 0.5V but here the positive sequence d-component only went down to 0.65V which is the residual voltage generating 0.15V of magnitude deviation, whereas the *q*-component stayed at zero.

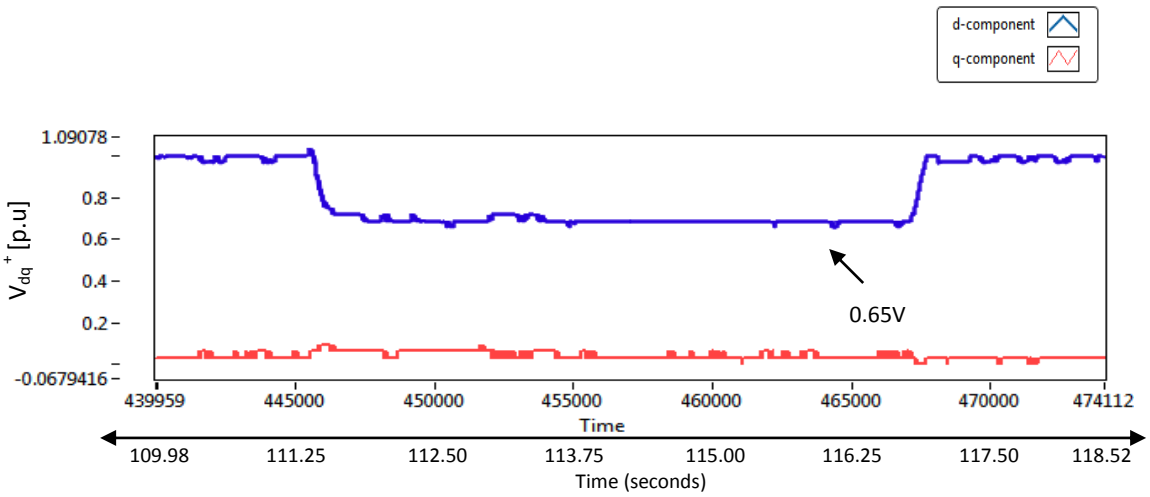


Figure 8.52: Positive *dq* components of the Type B Dip implemented

The dynamic response of the converter can be analysed by considering the following zoomed-in screen shots of the above figure 8.52:

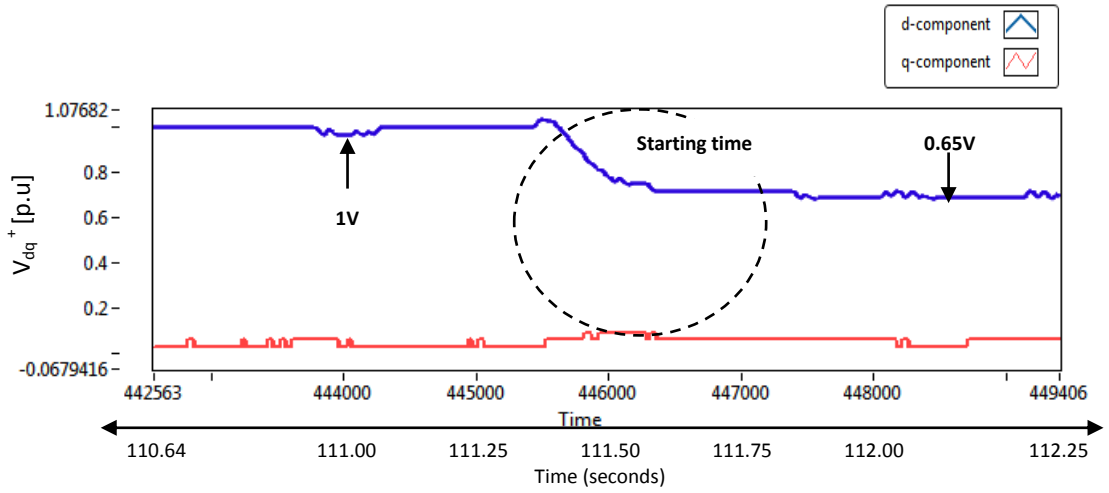


Figure 8.53: Start of the Positive *dq* Components of Type B Dip

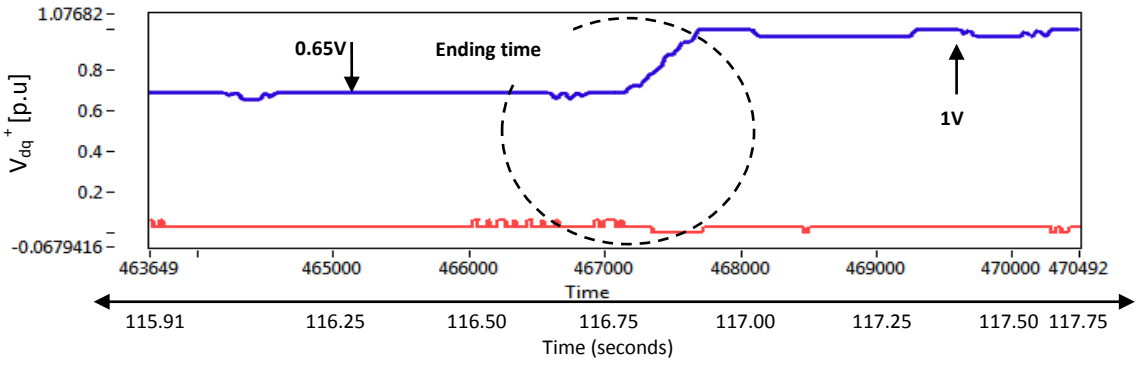


Figure 8.54: End of the Positive *dq* Components of Type B Dip

Figure 8.53 and 8.54 show almost the same settling time of 125ms for the dip. Similarly in figure 8.55 the negative *d*-component for balanced condition should stay at zero but here it touches 0.28V which is the residual voltage itself. Thereby generating 28% of magnitude deviation on the d component and the q-component has 5% of deviation respectively.

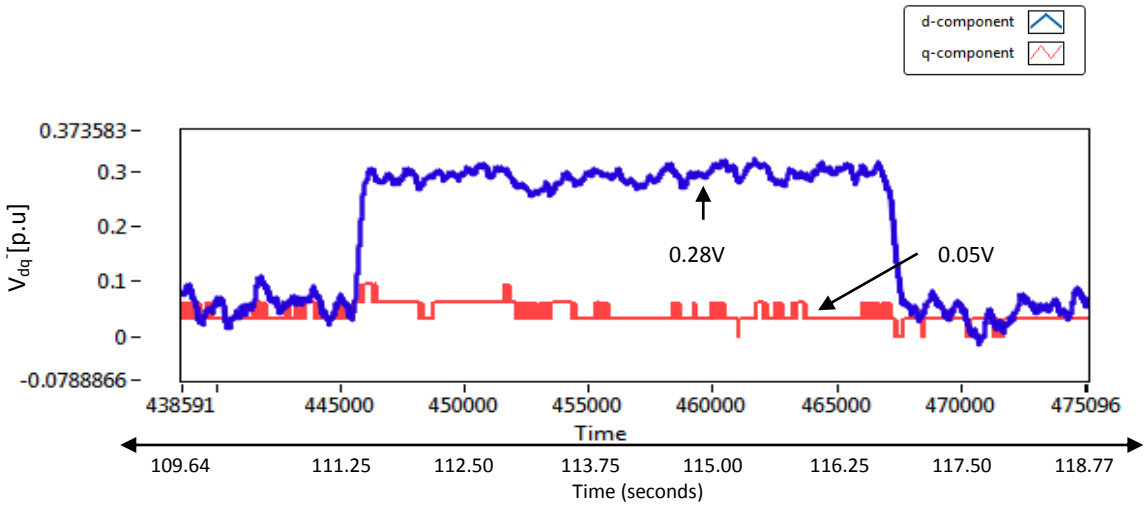


Figure 8.55: Negative *dq* Components with Type B Dip Implemented

The ripple in the above figure is due to the AC component discussed previously for figure 8.21. The dynamic response of the converter can be analysed from the following zoomed-in screen shots of the figure 8.55.

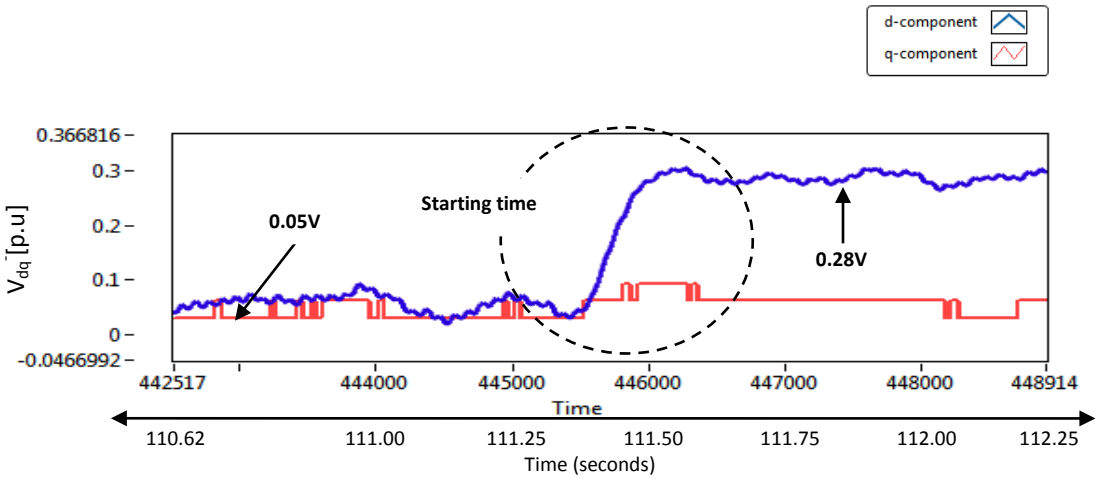


Figure 8.56: Start of the Negative *dq* Components of Type B Dip

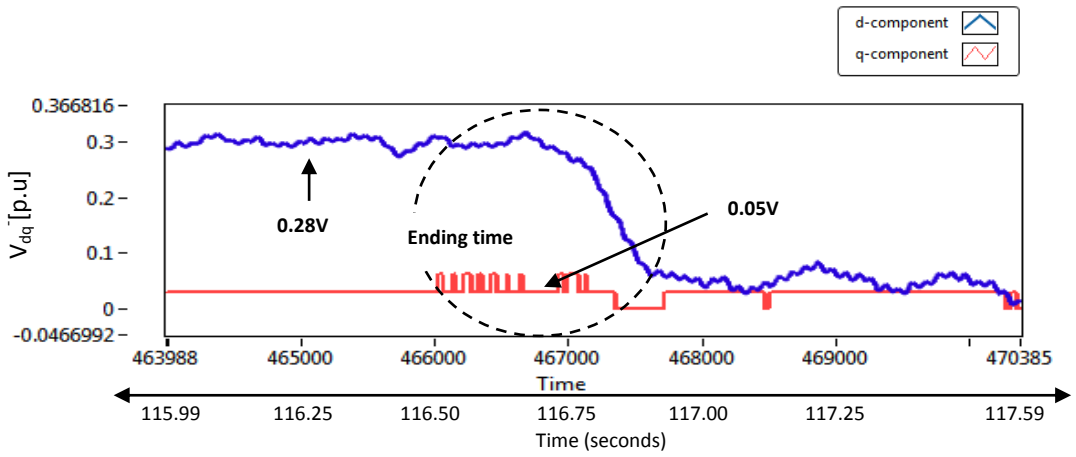


Figure 8.57: End of the Negative *dq* Components of Type B Dip

Figure 8.56 and 8.57 show settling time of 100ms at start and 50ms at the end of the dip.

➢ Type E Dip

This dip reduces the magnitude on two phases while maintaining the third at nominal voltage. The phase angles are maintained thereby allowing magnitude unbalance to be implemented as shown in chapter6, figure 6.18. Figure 8.58 shows the waveforms in which two phases has a lower magnitude than the third. Change in magnitude on phases A and C voltage can be seen.

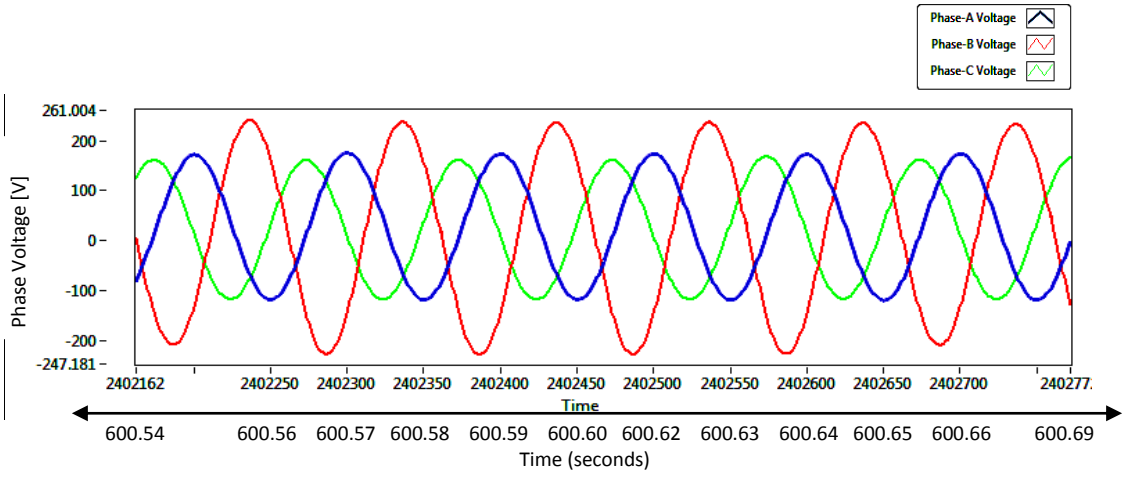


Figure 8.58: Type-E Dip Implemented

A 50% voltage dip was implemented. The figure above shows the correlation with figure 6.38. Experimental results can be further verified by means of a power quality analyzer. The output

waveforms of the emulator were captured by means of the analyzer for the Type E dip and are shown in figure 8.59 below.

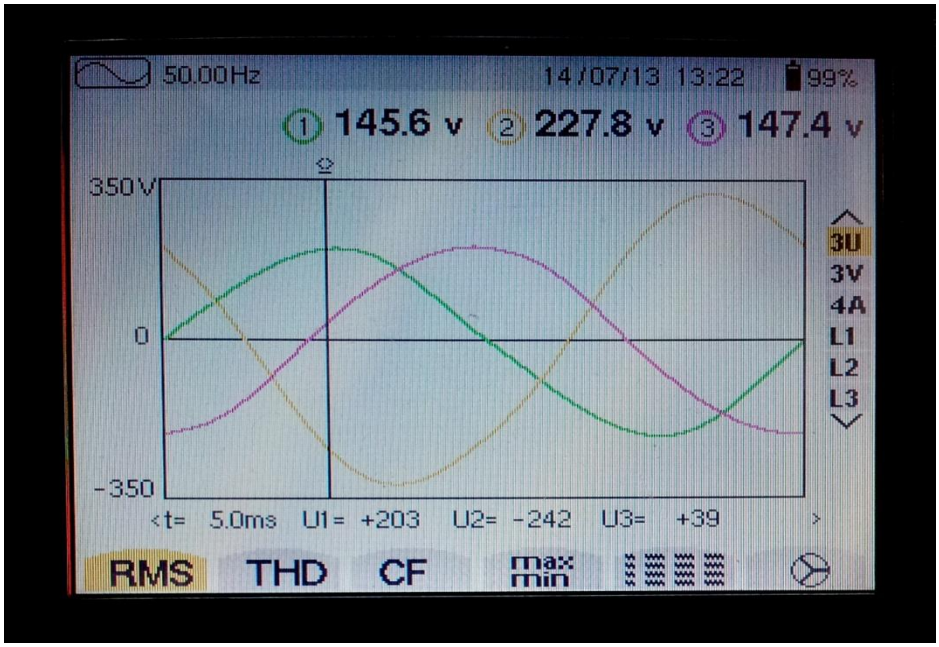


Figure 8.59: Type-E Dip from the Analyzer Output

THD was also checked with the analyzer and is shown in figure 8.60 below:

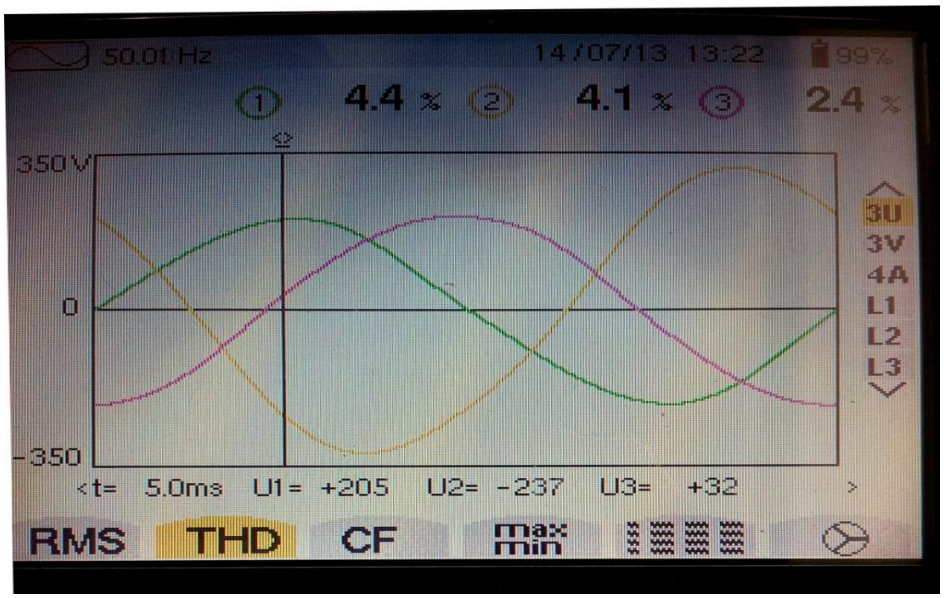


Figure 8.60: Percentage THD for the Type-B Dip from the Analyzer Output

As discussed earlier an unexpected phase unbalance was recorded which is shown in the figure below. Phase unbalance during Type E dip is shown in the figure below. For a perfectly balanced system, the in-phase angle should be 120° but here it is -73° and -143° respectively.

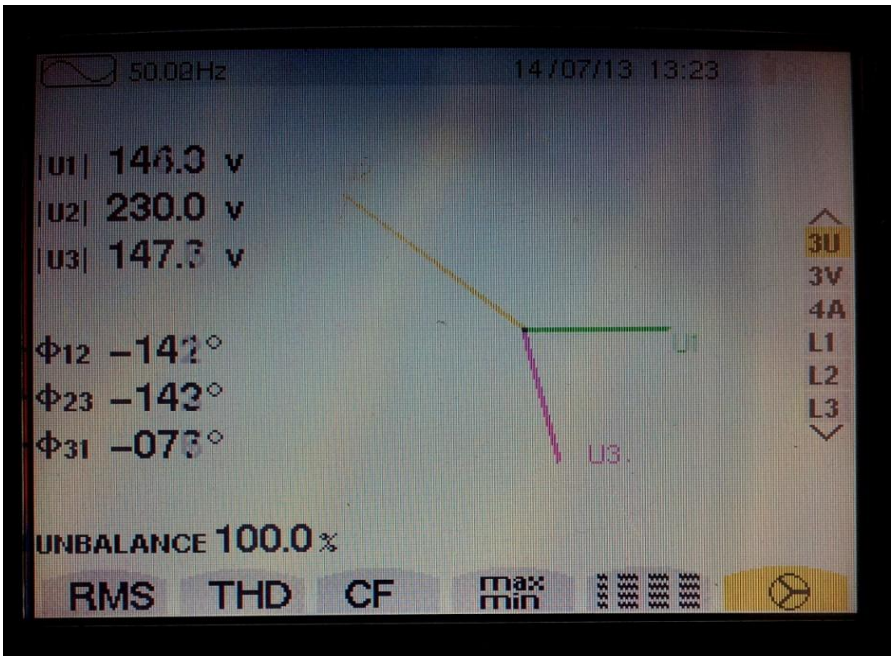


Figure 8.61: Phase Information for the Type-E Dip from the Analyzer Output

Three phase voltages are then converted into *dq* components in order to analyze the dynamic operation of the converter with this dip. Figures 8.62 and 8.65 show the measured positive and negative sequence *dq* voltages for the Type E dip implemented. Figure 8.69 shows positive sequence components. A 50% dip on two phases was applied which led to a 10% magnitude deviation. For a 50% symmetrical voltage dip the waveform should go to the half of the peak voltage i.e 0.5V but here the positive sequence *d*-component only went down to 0.6V which is the residual voltage generating 0.10V of magnitude deviation and the *q*-component stayed at zero. Moreover, it is noticed from the figure 8.52 and 8.62 that the positive *d*-component in the Type E has lower magnitude unbalance than the Type-B. From the results it is recorded to be 5%.

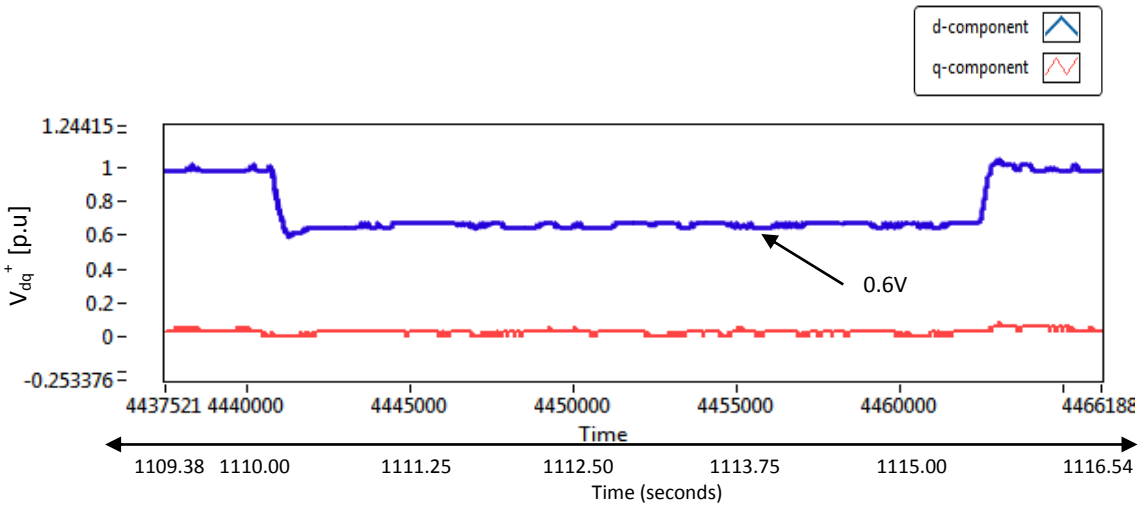


Figure 8.62: Positive *dq* Components with Type E Dip Implemented

The dynamic response of the converter can be analysed from the following zoomed-in screen shots of the above figure:

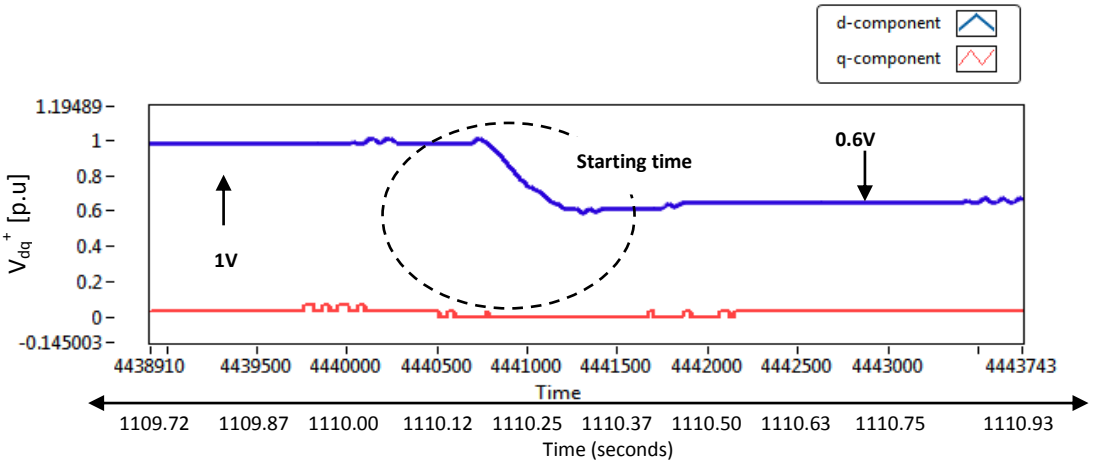


Figure 8.63: Start of the Positive *dq* Components of the Type E Dip

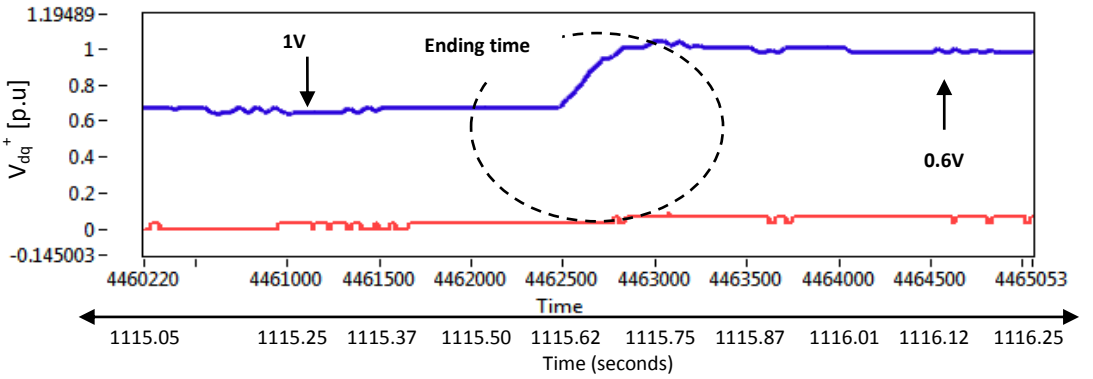


Figure 8.64: End of the Positive *dq* Components of the Type E Dip

Figure 8.63 and 8.64 show settling time of 110ms at the start and 100ms at the end of the dip. Similarly in figure 8.65 the negative *d*-component, for balanced condition or a symmetrical dip remains at zero but here it touches -0.13V which is the residual voltage itself. Thereby generating 13% of magnitude deviation and the *q*-component has 5% of deviation respectively.

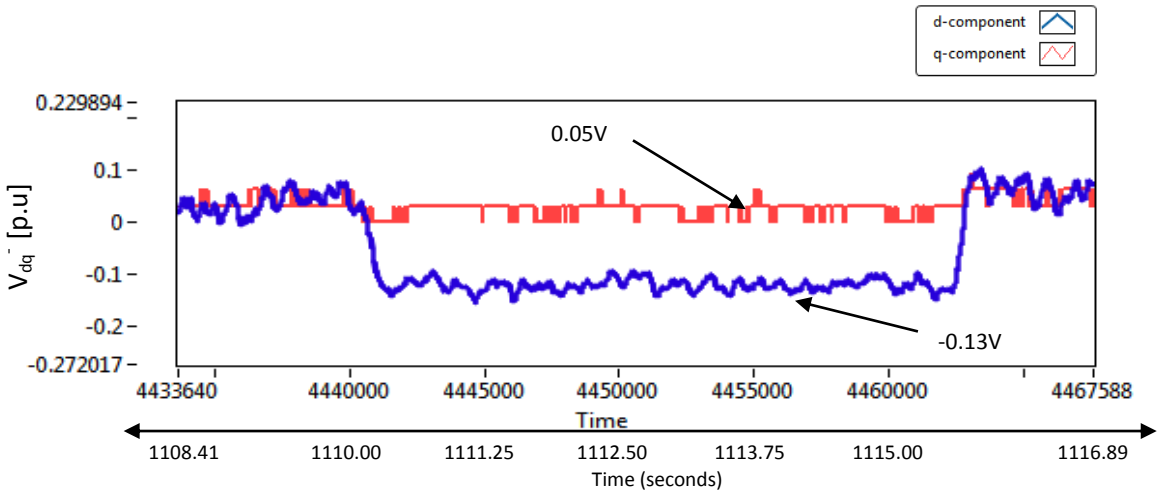


Figure 8.65: Negative *dq* Components of the Type E Dip Implemented

Dynamic response of the converter can be analysed from the following zoomed-in screen shots of the above figure 8.65.

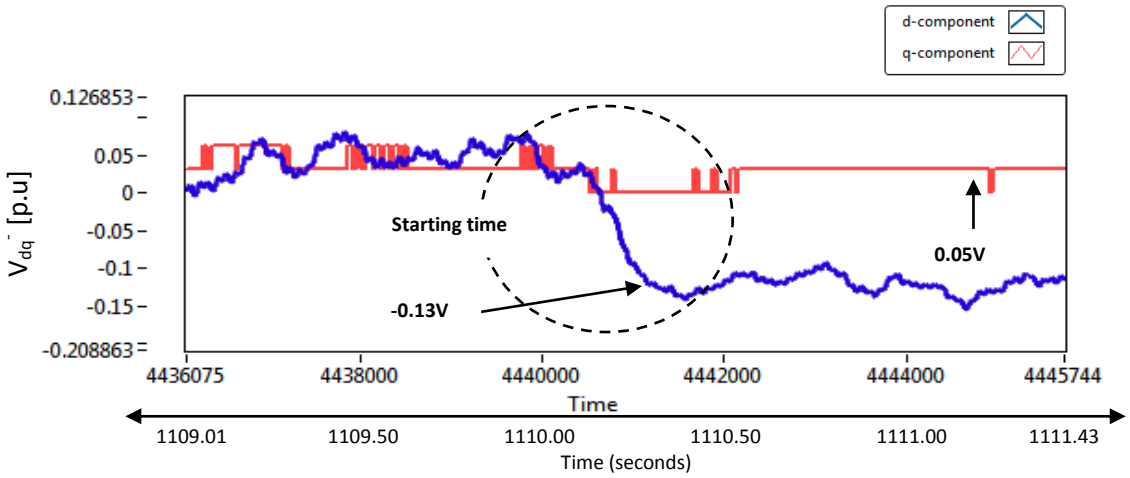


Figure 8.66: Start of the Negative *dq* Components of Type E Dip

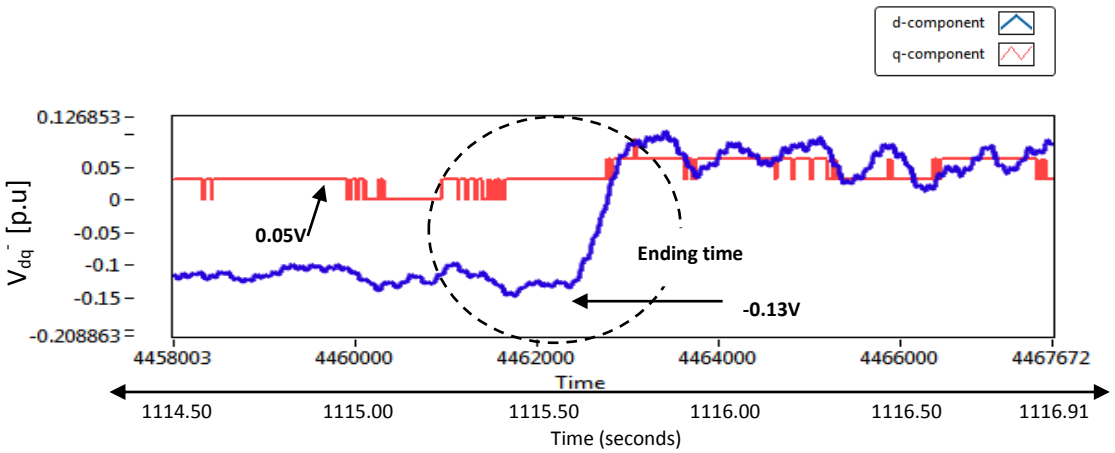


Figure 8.67: End of the Negative *dq* Components of Type E Dip

Figure 8.66 and 8.67 show a settling time of almost 300ms at the start and 200ms at the end of the dip. It can be concluded that the Type-E dip has a lower negative *d*-component deviation than the negative *d*-component of Type-B dip and it was 13%. Moreover the average dynamic response of the converter for all the positive sequence dips is 160ms, whereas for negative sequences it is inspected to be 90ms.

8.3.3.2. Voltage Swell/Overvoltage

This is a momentary increase of the voltage, beyond the normal tolerance for more than one cycle and is typically less than a few seconds. This increases the magnitude on all three phases. The phase angles are maintained thereby allowing symmetrical magnitude change to be implemented as shown in figure 8.68. In the figure below a 50% symmetrical overvoltage is implemented on the grid emulator's output.

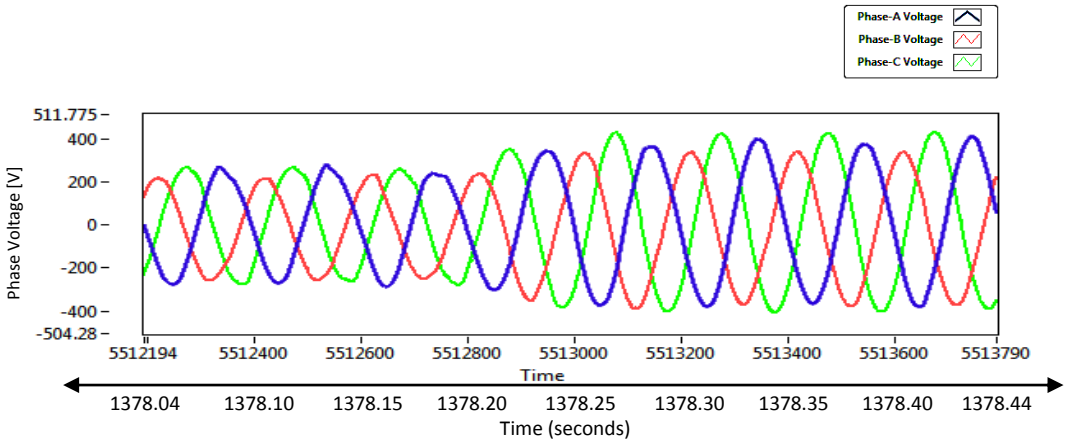


Figure 8.68: Symmetrical Overvoltage Implemented

In order to analyse the dynamic response, the three phase voltages are converted into *dq* components. 50% overvoltage is applied from the grid emulator. As it is a symmetrical overvoltage, there will be no negative sequence *dq* components. The positive *dq* waveforms are shown in figure 8.69

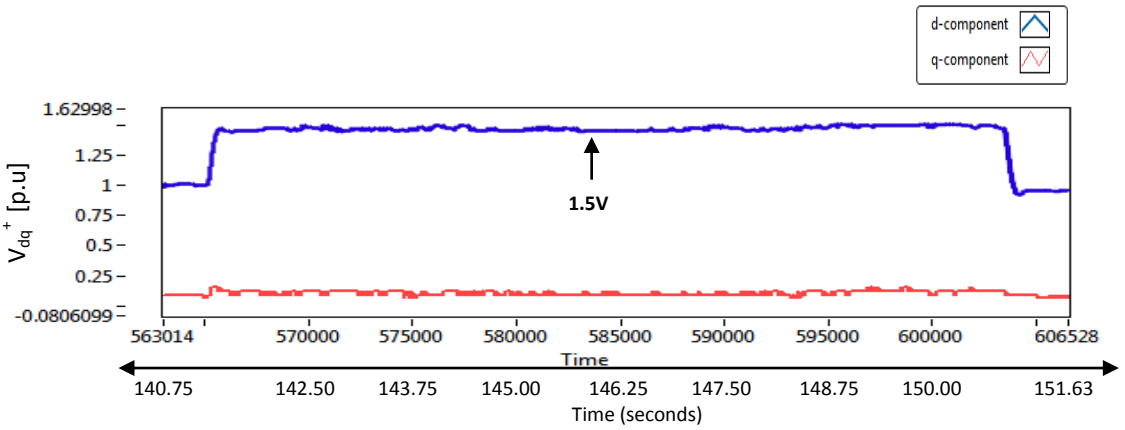


Figure 8.69: Positive *dq* components of the Symmetrical Overvoltage Implemented

Zoomed-in screen shots for the start and end of the overvoltage are shown below. Figure 8.70 shows the settling time of the overvoltage and i.e almost 80ms for both cases.

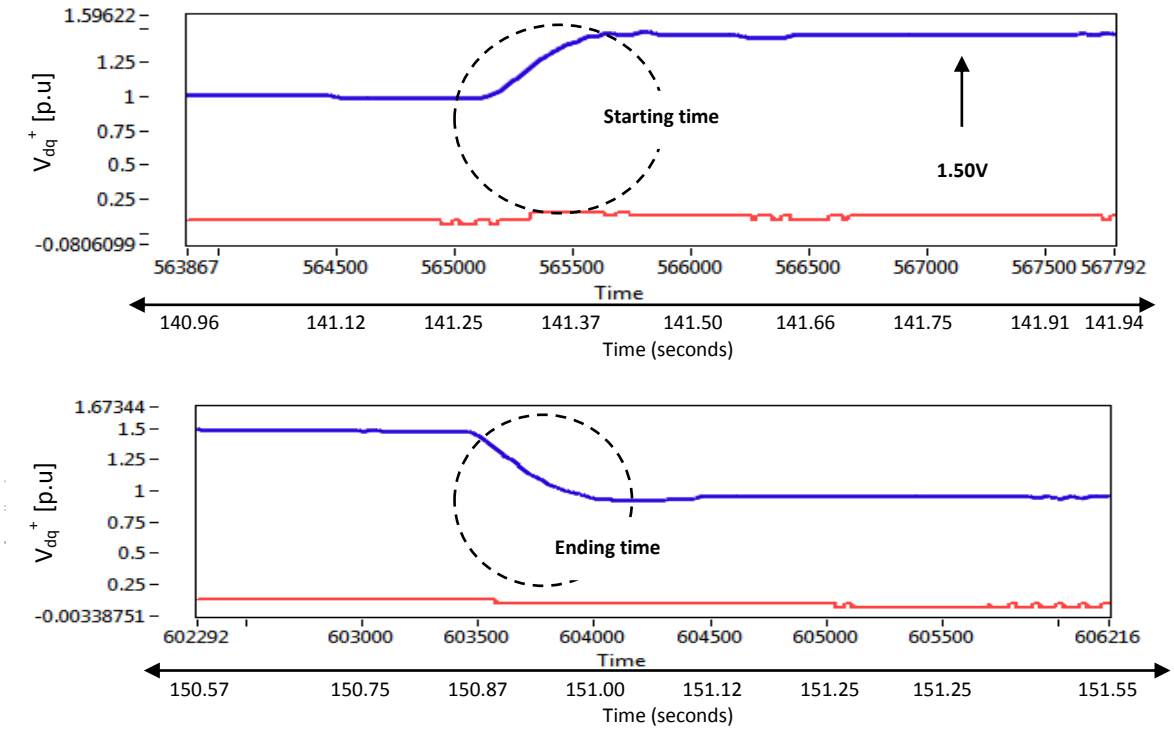


Figure 8.70: Zoomed-in Screen Shots of the Positive *dq* Components

8.4. Conclusion

The experimental results obtained in the laboratory have been presented and discussed in this chapter. The individual system components were tested individually to validate the correct operation of each part of the system. Subsequently, the Grid Emulator operated as expected. A thorough assessment of the dynamic response of both converters was conducted by analysing the experimental results. All voltage conditions discussed in chapter 6 were implemented successfully in experiments. It was concluded that the three-level converter showed an overall better performance with less THD as compared to the two-level converter. In inverter mode of operation and considering dip generation only, the table below shows that the average dip-injection and dip-recovery time of both converters. It shows that the three-level converter is slower than the two-level converter i.e approximately 30% in terms of positive sequence, whereas it is 50% faster in case of negative sequences. On the other hand it gives three times less magnitude deviation as compared to the two-level converter.

Table 8.1: Performance Analysis of the two converters in inverter mode of operation

Dip Type	Two-Level Inverter		Three-Level Inverter	
	Avg Response Time	%Magnitude Deviation	Avg Response Time	% Magnitude Deviation
A	50ms	0%	125ms	0%
B	+ve seq 65ms	+*d* : 20% +*q* : 0%	+ve seq 150ms	+*d* : 15% +*q* : 0%
	-ve seq 125ms	-*d* : 28% -*q* : 5%	-ve seq 75ms	-*d* : 28% -*q* : 5%
E	+ve seq 83ms	+*d* : 5% +*q* : 0%	+ve seq 100ms	+*d* : 10% +*q* : 0%
	-ve seq 150ms	-*d* : 90% -*q* : 5%	-ve seq 100ms	-*d* : 13% -*q* : 5%

CHAPTER 9

CONCLUSIONS AND RECOMMENDATIONS

9.1. Conclusions

This thesis discusses methods of implementing voltage unbalance in a network of renewable energy systems. The objective is to make a grid emulator which would be able to generate disturbed voltage conditions. Analysis and implementation is presented. Based on the findings of the thesis, the following conclusions can be drawn:

- The concept of the two converter topologies was discussed in detail, which differs in terms of operating behavior and/or strengths and weaknesses. It was determined that the PWM switching time calculation for the three-level converter was extensive and cumbersome but it gives well defined harmonic spectrum.
- A higher order LCL filter was designed to eliminate the current ripples and switching frequency harmonics using small inductance values. It was deduced that at high frequency operation, the LCL filter has a larger current harmonic attenuation for the same value of inductance used in an L-filter. The experimental results confirmed that the resonance was removed.
- For unbalanced conditions, sequence component filtering was done. The filter included in the model was used to design the controllers for the current and voltage control loops. The control loops were tested in simulations and experimentally. Voltage oriented control was implemented because of its independent control on active and reactive current components which corresponds to a direct control of the power flow.
- A model of the grid emulator was developed in order to design the controllers for the voltage control. Both grid and load side controls were investigated. The current and voltage loop controllers were tested in simulation and experimentally.

- Unbalanced voltage conditions were tested in simulations and experimentally. It can be concluded from the results that the system control was able to regulate voltage effectively during such conditions. Furthermore it was investigated that the overall injection and recovery time of the disturbance for the three-level converter is faster than that of the two-level converter with less THD value.

9.2. Recommendations

- The grid emulator can be further enhanced by implementing more voltage conditions in the system such as phase unbalance and harmonics generation.
- Passive load can be replaced by a generator as a load for bi-directional power flow analysis.
- Better matched and more ideal components to construct the grid-filter can be considered. This can improve the performance of the grid-side converter whilst decreasing current ripple during unbalance.
- Phase unbalance was detected in the three-phase voltage vectors from the spectrum analyzer. It might have occurred because of the in-line inductance or from the unbalanced load. This unwanted unbalance can be eliminated by further in-depth analysis of both situations.
- More improved control schemes can be implemented for a fast dynamic response.
- Modular multi-level converter topology can be considered for advanced operations with improved THD. It offers low expense of filters, simple scalability and redundancy.

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APPENDIX A

Dwell time calculation of the reference voltage vector in sectors 2-6 for the three-level converter is given in the tables below:

Sector 2

Region / Time	1	2	3	4
S1A	$T_a + \frac{T_c}{2}$	0	$\frac{T_c}{2}$	$\frac{T_b}{4} + \frac{T_c}{2}$
S2A	0	$\frac{T_a}{2} + T_c$	$\frac{T_a}{2}$	$\frac{T_b}{2} + \frac{T_a}{2}$
S1B	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + T_c$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{2} + \frac{T_c}{2}$
S2B	0	0	0	$\frac{T_b}{4}$
S1C	0	0	0	$\frac{T_b}{2}$
S2C	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + T_c$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{4} + \frac{T_c}{2}$

Sector 3

Region / Time	1	2	3	4
S1A	0	$\frac{T_b}{2}$	0	0
S2A	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{4} + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + T_c$
S1B	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{2} + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + T_c$
S2B	0	$\frac{T_b}{4}$	0	0
S1C	$T_a + \frac{T_c}{2}$	$\frac{T_b}{2} + \frac{T_c}{2}$	$\frac{T_c}{2}$	0
S2C	0	$\frac{T_a}{2} + \frac{T_b}{4}$	$\frac{T_a}{2}$	$\frac{T_a}{2} + T_c$

Sector 4

Region / Time	1	2	3	4
S1A	$\frac{T_b}{2}$	0	0	0
S2A	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$T_a+T_b+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+T_c$
S1B	$\frac{T_b}{2}+\frac{T_c}{2}$	$T_a+\frac{T_c}{2}$	$\frac{T_c}{2}$	0
S2B	$\frac{T_a}{2}+\frac{T_b}{4}$	0	$\frac{T_a}{2}$	$\frac{T_a}{2}+T_c$
S1C	$\frac{T_a}{2}+\frac{T_b}{2}+\frac{T_c}{2}$	$T_a+T_b+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+T_c$
S2C	$\frac{T_b}{4}$	0	0	0

Sector 5

Region / Time	1	2	3	4
S1A	0	$T_a + \frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2} + \frac{T_c}{2}$
S2A	$\frac{T_a}{2} + T_c$	0	$\frac{T_a}{2}$	$\frac{T_a}{2} + \frac{T_b}{4}$
S1B	0	0	0	$\frac{T_b}{2}$
S2B	$\frac{T_a}{2} + T_b + T_c$	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{4} + \frac{T_c}{2}$
S1C	$\frac{T_a}{2} + T_b + T_c$	$T_a + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + T_b + \frac{T_c}{2}$	$\frac{T_a}{2} + \frac{T_b}{2} + \frac{T_c}{2}$
S2C	0	0	0	$\frac{T_b}{4}$

Sector 6

Region / Time	1	2	3	4
S1A	$\frac{T_a}{2}+T_b+T_c$	$\frac{T_a}{2}+\frac{T_b}{2}+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+\frac{T_c}{2}$	$T_a+T_b+\frac{T_c}{2}$
S2A	0	$\frac{T_b}{4}$	0	0
S1B	0	$\frac{T_b}{2}$	0	0
S2B	$\frac{T_a}{2}+T_b+T_c$	$\frac{T_a}{2}+\frac{T_b}{4}+\frac{T_c}{2}$	$\frac{T_a}{2}+T_b+\frac{T_c}{2}$	$T_a+T_b+\frac{T_c}{2}$
S1C	0	$\frac{T_b}{2}+\frac{T_c}{2}$	$\frac{T_c}{4}$	$T_a+\frac{T_c}{2}$
S2C	$\frac{T_a}{2}+T_c$	$\frac{T_a}{2}+\frac{T_b}{4}$	$\frac{T_a}{2}$	0

APPENDIX B

The Interfacing of Labview with Multisim is shown with the help of the figures below. A converter model is first implemented in Multisim and then linked up in Labview using Co-Simulation method. A simulation code is shown in the figures B.1 and B.2 followed by the complete hardware code pictures:

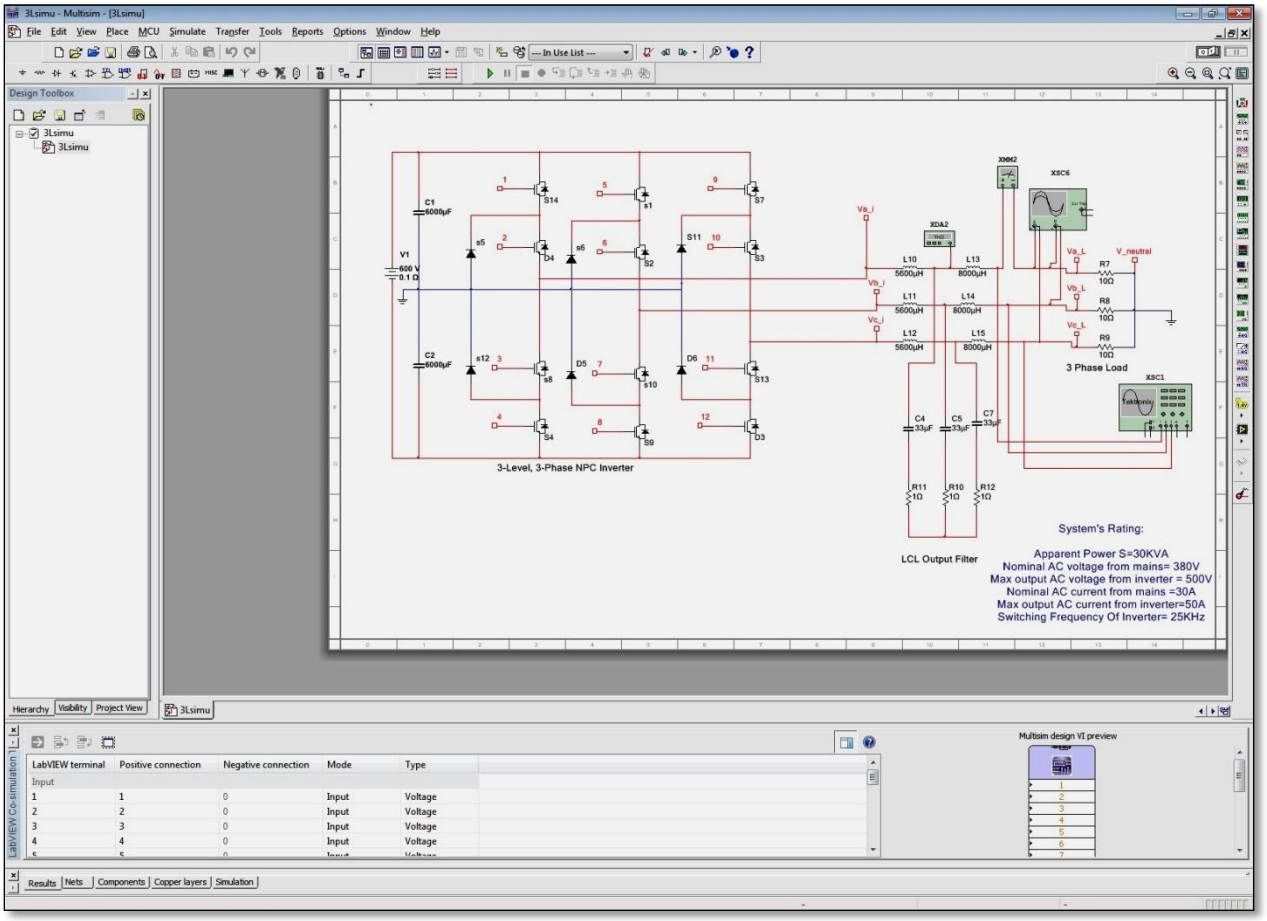

Figure B.1: Implementaion of the Three-Level Converter in Multisim

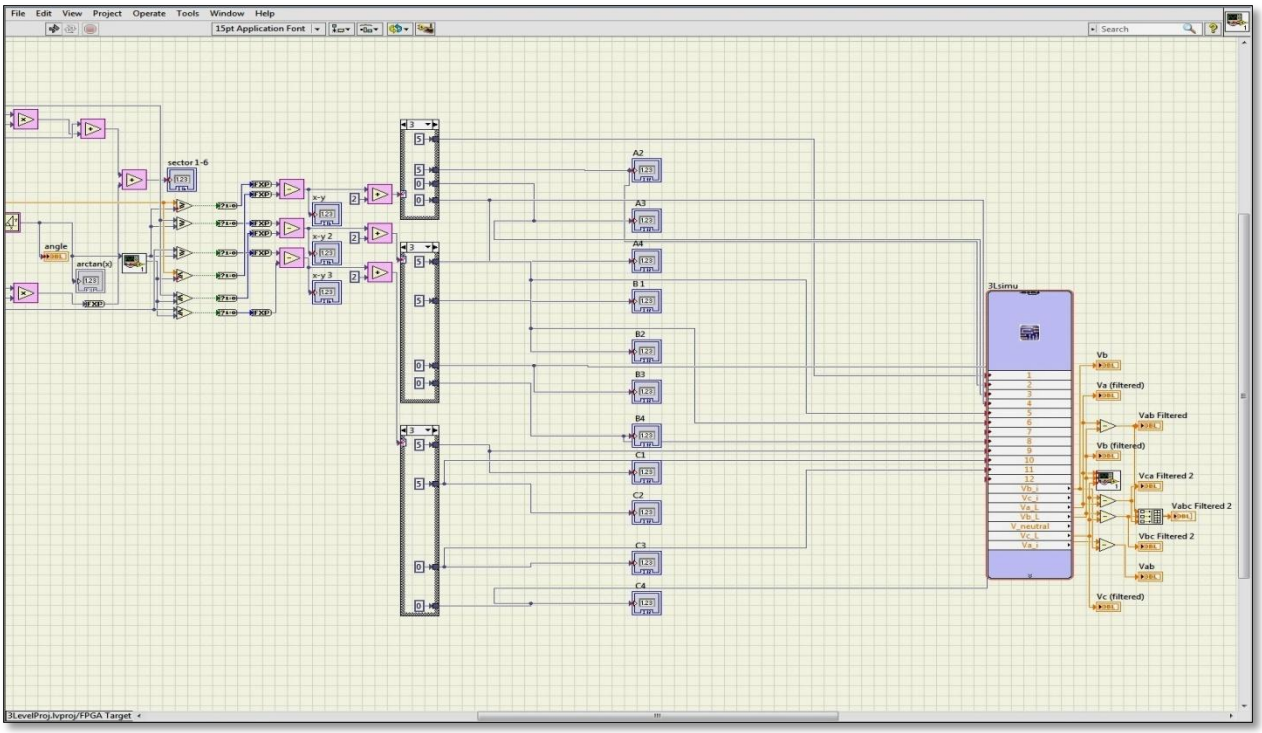

Figure B.2: Co-simulation: Multisim Model Interfaced with Labview Model

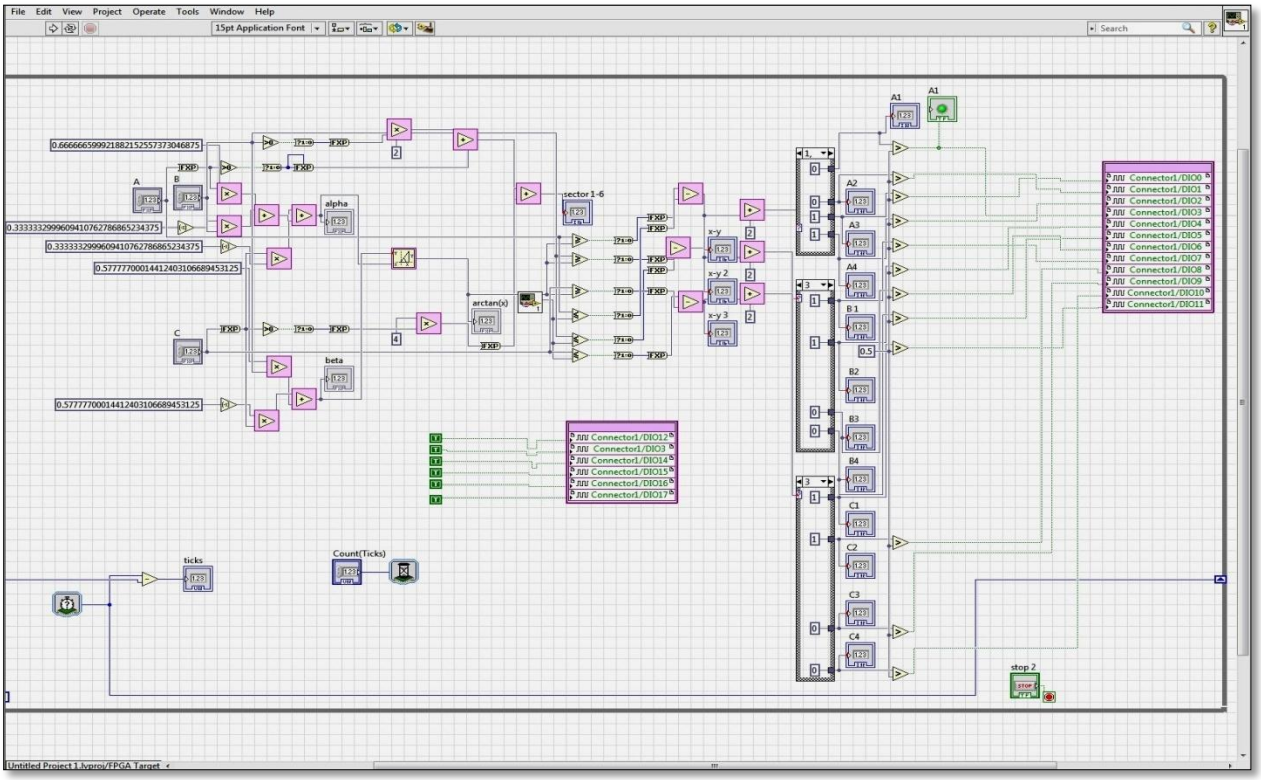

Figure B.3: Calculatoin of αβ values and Sector Selection

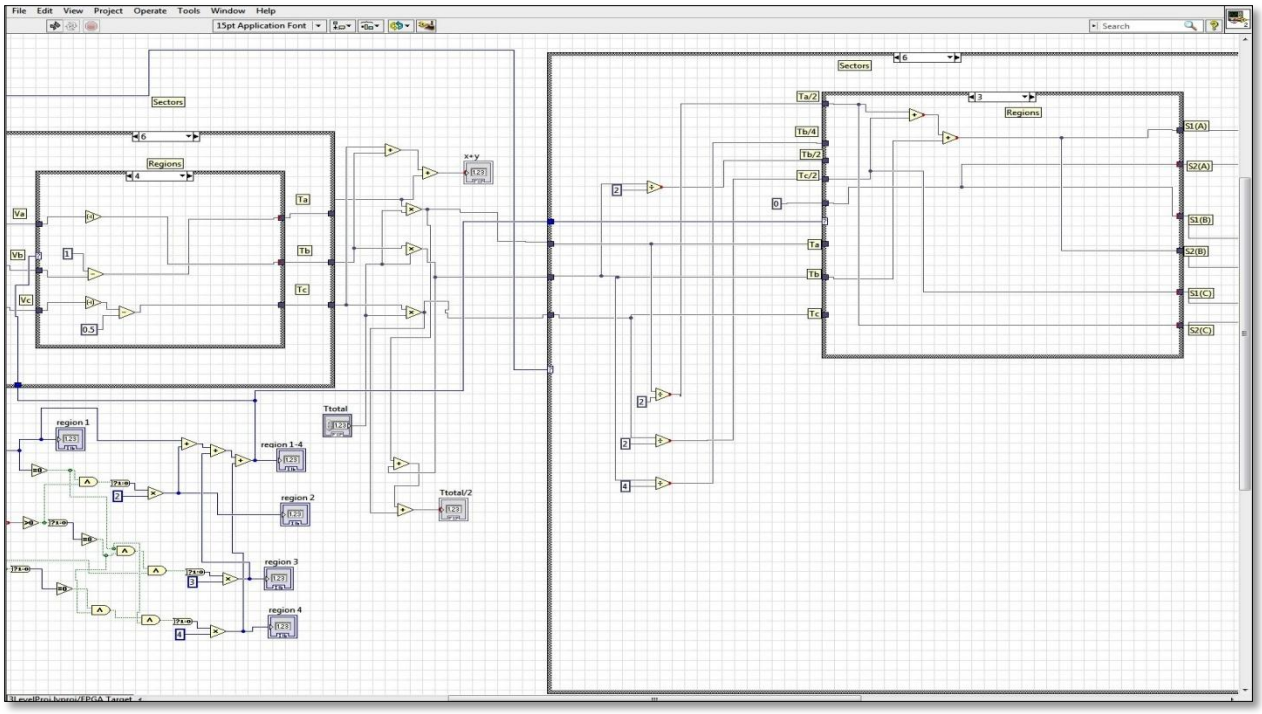

Figure B.4: Dwell Time Calculation in Sectors and Regions

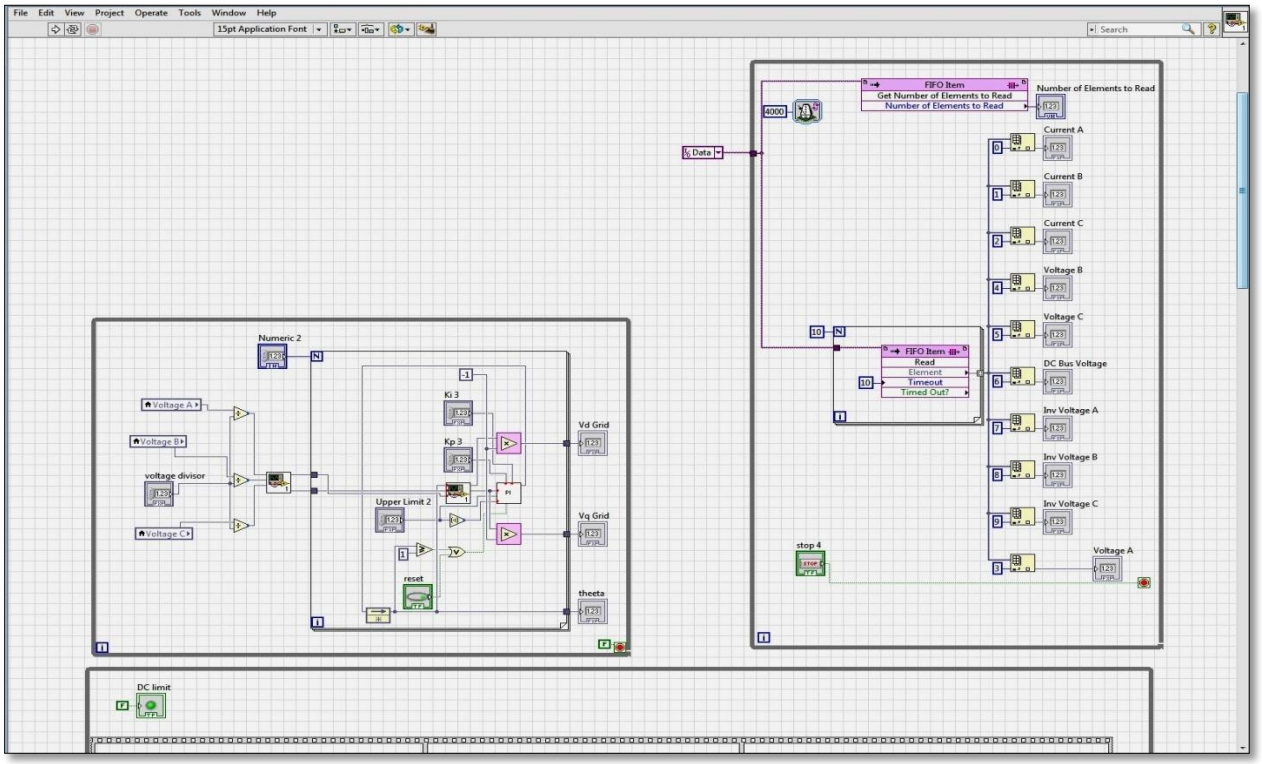

Figure B.5: PLL Calculation and Analog Data Reading

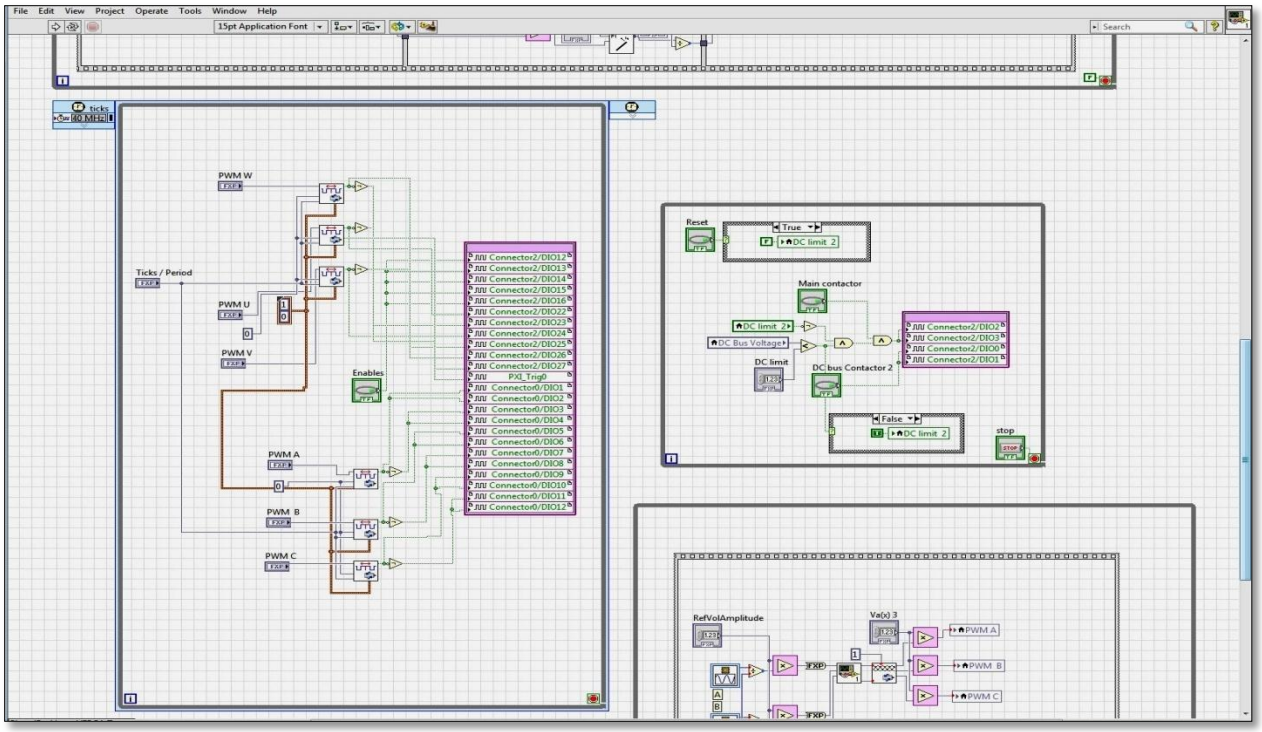

Figure B.6: FPGA Triggering for Switching and Contactors

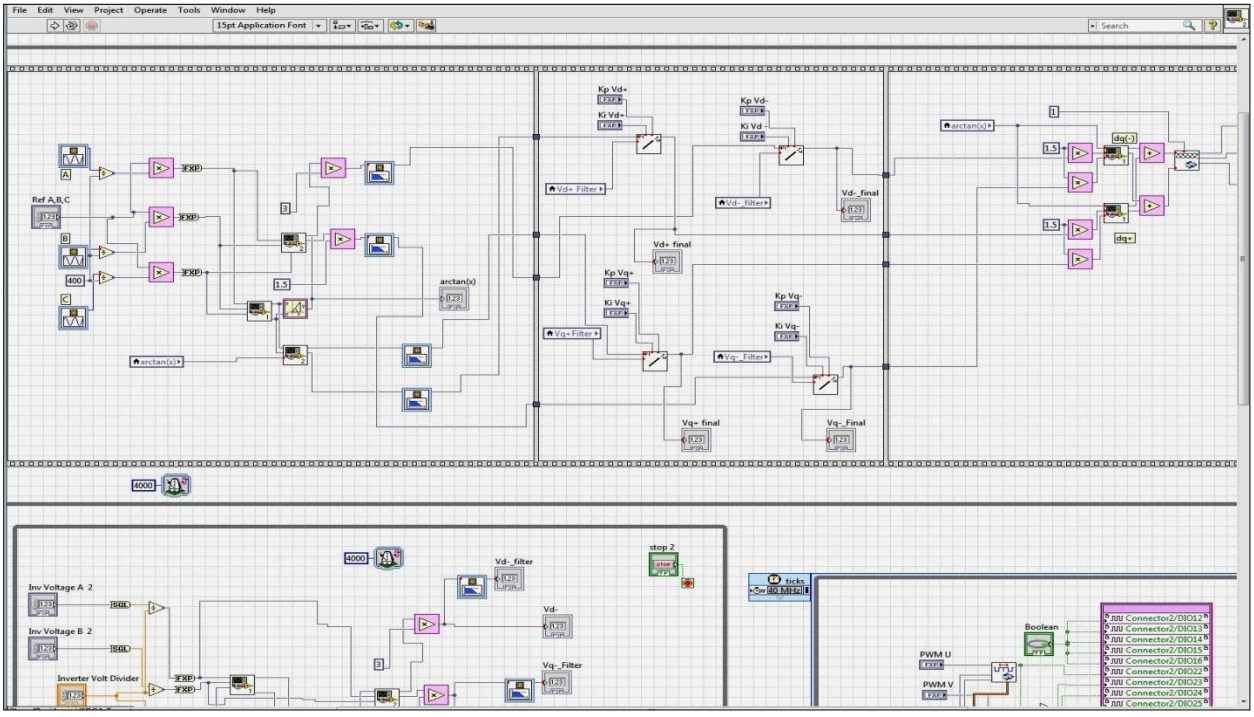

Figure B.7: Reference Values with Extraction of dq Components

APPENDIX C

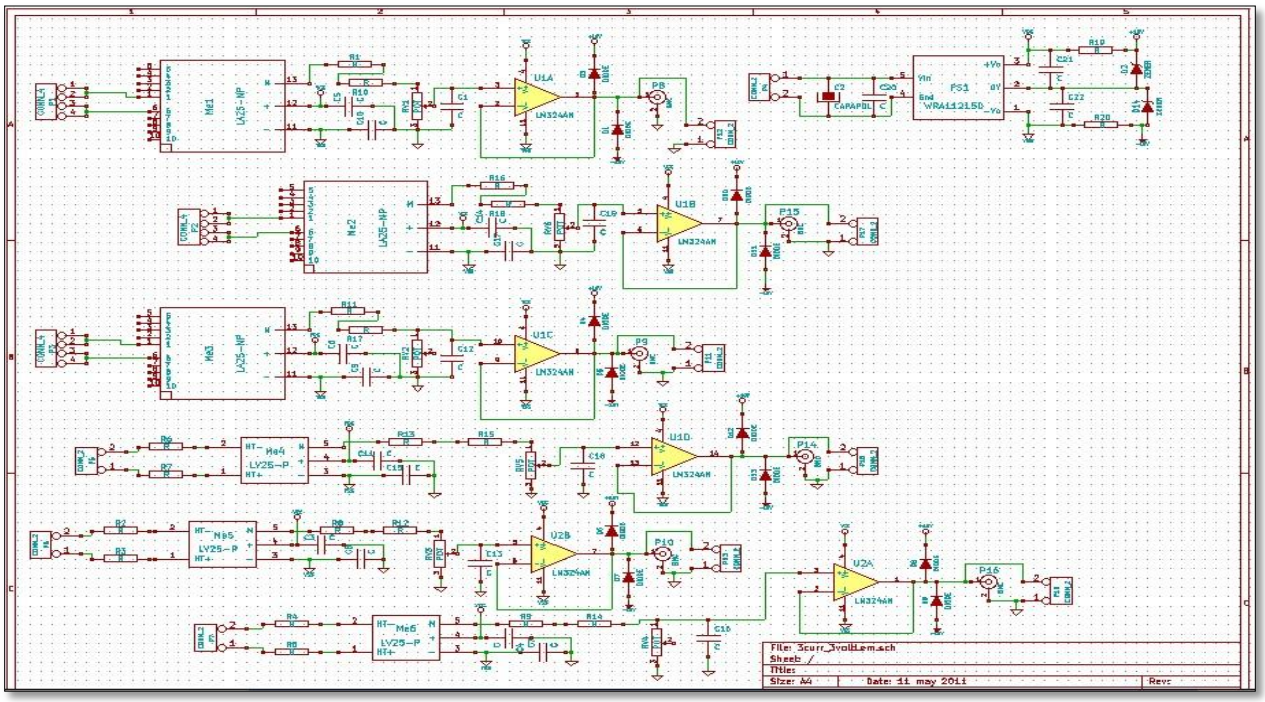

Figure C.1: LEM Board Circuit Diagram

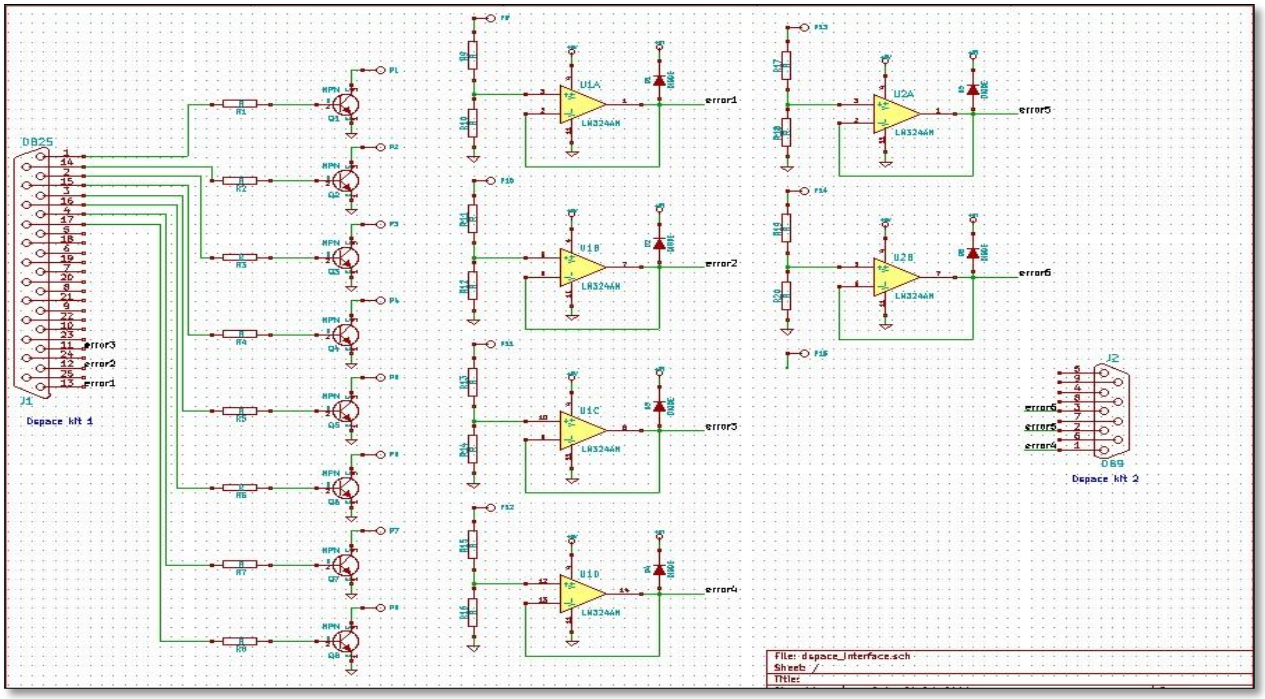

Figure C.2: Relay and Error Signal Circuit Board

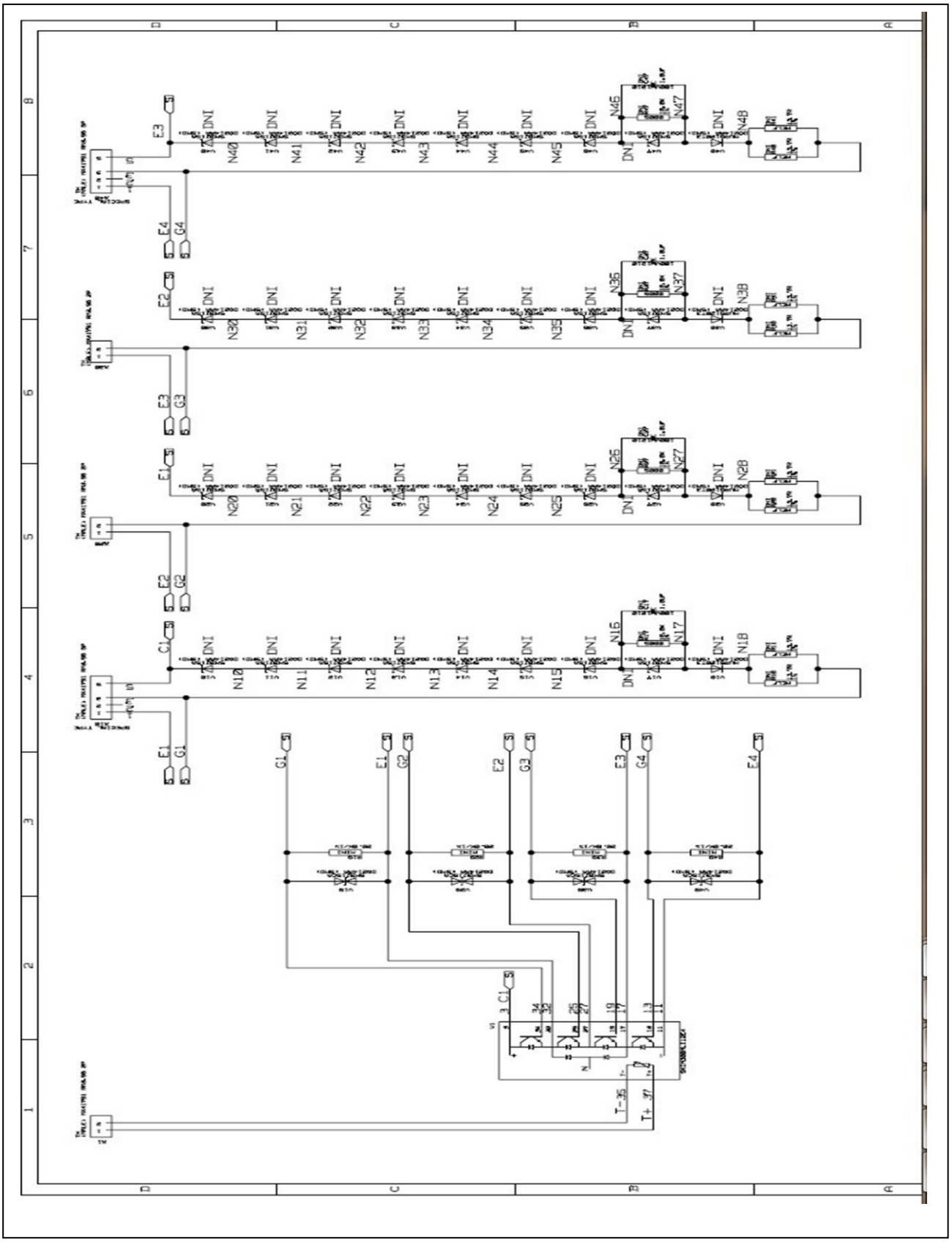

Figure C.3: skim200MLI-12E4 Circuit Diagram